STUDY OF STATIC INVERTERS

Final Report

June 15, 1966

R. G. Klimo W. V. Peterson R. J. Resch

CONTRACT NUMBER NAS 9-5581

CONTROL NUMBER 508-8038

Prepared For

National Aeronautics and Space Administration
Manned Spacecraft Center
General Research Procurement Branch
Houston, Texas 77058

TRW EQUIPMENT LABORATORIES
A DIVISION OF TRW INC. • CLEVELAND, OHIO 44117

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SUMMARY

This document is the Final Report for the work performed on Contract Number NAS-9-5581. The object of the program was the study of static inverters. Specifically the effort was directed to the devising of an advanced circuit approach for the design of an optimum light weight single phase static inverter. The report covers the period from January 15, 1966 to June 15, 1966 during which a basic approach was selected from two initial concepts and investigated in detail. The selected inverter was designed in sufficient detail to permit the completion of a realistic packaging effort which yielded a compact, producible, and reliable inverter configuration.

1. INTRODUCTION

The work carried out by this program was the Study Program or Phase One portion of the static Inverter Development requirement described by NASA-MSC-RFP BG 731-31-6-19 P. The goal of the program was to devise an advanced modular-type static inverter having the following characteristics:

1) Reliability
2) Low weight
3) High efficiency
4) Compatibility with a fuel cell source
5) Compatibility with a wide variety of AC loads
6) Capability of being interconnected with identical modules in three phase and/or parallel hookups

At the initiation of the program two basic inverter concepts were investigated and evaluated. The concepts were called the Phase Angle Modulated or PAM inverter and the Pulse Width Modulated or PWM inverter. Each inverter systemwas nearly identical in terms of performance, parts count, and weight. The PWM inverter system was chosen for detail study after evaluation because of fewer power-switching semiconductors, less audio noise generation and less functional complexity.

Each inverter concept was based on the generation of a sinusoidal 400 cycle output voltage by means of high-frequency pulse width modulation techniques. The purpose for using the high frequency techniques was to eliminate the rather heavy 400 cycle power transformers used in conventional inverter designs and also to raise the distortion components to a high frequency which would permit the use of rather light weight filtering methods. Each inverter system yielded rather light weight and low energy storage designs (in terms of internal filtering requirements) when operated from low impedance power sources.

The application of the basic inverter designs to rather high impedance power sources such as fuel cell sources introduced major design complications which added components and weight to the inverter. The solution to this problem is presented in the report.

The design objectives of the static inverter are summarized in the following table.

Input Voltage:

28 plus or minus 4 volts, 0.5 ohm source impedance.

Output Voltage:

115 volts rms.

Regulation:

plus or minus 1 percent.

Frequency:

400 cps plus or minus 2 percent when free running. Plus or minus 1 percent when synchronized with a 6400 cps signal.

Output Power:

500 VA continuous.
750 VA for 10 minutes.

Power Factor:

0.65 lagging to 0.8 leading at all levels, 0.8 to 0.1 leading for 0 to 30 percent load.

Short Circuit:

14 amps for twenty seconds, self-protecting and automatic recovery.

Harmonic Distortions:

5% total

Efficiency:

80 percent at rated load
60 percent of 40% rated load

Weight:

15 pounds

A detailed specification is appended at the end of the report.

II BASIC SYSTEM DESCRIPTIONS

In this section the PAM and PWM inverters will be described.

A. Phase Angle Modulated (PAM) Inverter

The inversion method described here is basically a special type of high frequency pulse width modulation. The high frequency repetition rate, 7.5 kilocycles in this case, is much higher than the desired 400 cps output frequency. The 400 cps signal is used to first modulate and then demodulate the 7.5 KC.

The basic concept of the inverter can best be described with the assistance of the block diagram shown in Figure 1. This diagram describes the essential areas of the PAM Inverter.

The inverter consists of two parallel-type power inverters (high power switching amplifiers). The switching elements are parallel combinations of high-speed transistors in a push-pull configuration. The paralleling of the transistors permits safe overloading of the inverter without incurring transistor damage. One of these, called the "master", runs at a constant frequency of approximately 7.5 KC. The second one, called the "slave", also runs at 7.5 KC but its phase angle is controlled by a modulator operating on the high frequency square wave drive signal. The phase angle modulation is controlled such that in the absence of modulation signals, the two inverters are 180° out of phase and their sum is zero. When a modulation signal is present (from the sine wave reference), the phase angle of the modulated inverter voltage is reduced with respect to the unmodulated inverter. The shape of the modulating signal is a rectified sine wave because the modulated high frequency square wave can only contain amplitude information. The polarity information is re-inserted by the demodulator. The sum of the modulated and unmodulated square wave inverter voltage is a triple valued (+E, O, -E) pulse-width modulated train of high frequency pulses. Figure 2 illustrates this principle.

It can be seen from Figure 2 that the pulse width of the summed high frequency square waves is a proportional function of the rectified modulating signal. At the point in the circuit represented by Figure 2 the wave form has two important characteristics; a high-power level, but at a high frequency (7.5 KC) and a modulation or information characteristic which is proportional to the amplitude of a modulating signal.

Therefore, if the modulating signal is sinusoidal, the pulse widths will follow the amplitude of the modulation signal in a rectified sinusoidal manner. Figure 3 presents the waveforms with a 400 cps sinewave modulating signal. A demodulator must now be used to reconstruct the 400 cps sinewave information from the high frequency, high-power pulse width modulated waveform. The demodulator used in this inverter is a special type of keyed rectifier. The keying signals (sinewave reference and the high frequency square wave drive signal) control the demodulator and cause it to produce alternate positive and negative bunches of width modulated pulses at the 400 cps rate. A frequency doubling of the 7.5 KC also takes

place because of the full-wave nature of the demodulator. This raises the high frequency rate of the width modulated pulses to 15 KC permitting the use of a lighter and more efficient filter. Figure 3 illustrates the waveforms associated with the demodulator.

From the above explanation it is evident that power conversion from DC to 400 cps AC has been accomplished by using phase angle modulation of high frequency which utilizes light weight wound components. Also, the demodulator converted the high frequency waveform to a 400 cps waveform with only very high frequency distortion components which simplified the filter problem. The simple filter utilized also requires minimum energy storage which increases the regulation response time of the inverter.

The special demodulator referred to above is not a simple keyed rectifier but rather a keyed AC switch which permits bilateral power flow. This means the inverter can pump power backwards into the DC source (without storing it in an output filter) which is essential for reactive loads. This ability permits the inverter to drive all power factor loads.

B. Pulse Width Modulated (PWM) Inverter

The basic PWM Inverter block diagram is presented in Figure 4. It consists of a DC to DC converter and a transformerless inverter with the associated logic circuits.

A more detailed block diagram is presented in Figure 5 and briefly briefly described below.

The first part consists of a DC-DC converter and its associated logic circuitry. The DC-DC converter is used to step up the source voltage to a high DC voltage level (200 V_{DC}) that is compatible with the PWM power stage. Regulation of the AC output voltage against source variations is provided by the DC-DC converter. This is accomplished by feeding back an error signal which phase shifts one output square wave with respect to a second fixed output square wave resulting in a rectified quasi-square wave whose conduction angle depends on the error signal. The DC-DC converter operates at 20 KC in order to reduce its size and weight by using ferrite core material for all the transformers.

The second part consists of the low level logic circuitry required to generate the proper pulse width modulated waveforms that are required by the inverter power stage. A 400 cycle square wave, generated by the synchronizer circuit, is sent to the current reference and attenuator circuits. Current overload protection is provided in these circuits by reducing the amplitude of the square wave to zero. A band pass filter is used to extract the fundamental or 400 cycle component from the square wave. The sine-wave is then buffered and split into two out of phase voltages by means of a transformer. The resulting sinewaves are modulated by a 7.5 KC carrier frequency whose wave shape is triangular. The modulated sinewaves are then converted into naturally sampled pulse width modulated waveforms in the two slicer amplifiers. These two pulse width modulated waveforms whose 400 cycle components are 180° out of

phase are amplified in the driver stages which distribute them to the appropriate power switch segments in the inverter power stage.

The third part consists of a bridge inverter power stage and its AC filter. The bridge inverter power stage has high speed power transistors connected in each of its four switch segments. Two of these switch segments are connected to the positive line of the DC-DC converter while the other two are connected to the negative line. One driver circuit is used to control one positive and one negative switch segment. The two pulse width modulated waveforms from the driver circuits are subtracted in this bridge inverter power stage resulting in a difference waveform across the AC output filter. This difference waveform contains the 400 cycle component and the second and higher harmonics of the carrier frequency and their associated sidebands. The AC output filter suppressed these high frequency components allowing only the 400 cycle power frequency to appear across the load.

Figure six illustrates the waveforms developed by the inverter. This inverter approach, like the PAM system, has the following advantages.

1. No heavy 400 cycle output power transformer is required.

2. A light weight AC filter can be used since it is only required to suppress the second and higher harmonics of the carrier frequency and their sidebands.

3. The conversion efficiency of the pulse width modulated inverter power stage and AC filter is high (approximately 90%).

C. Multi-Module Operation - Three Phase and/or Parallel Connection

Regardless of which basic inverter approach is selected it is mandatory that either inverter type be a "Building Block". Extra low level logic circuits are required to provide the necessary signal processing which enables the basic single-phase module to function in parallel with other modules or in one leg of three phase systems. Furthermore, this logic must be capable of synchronizing the module to an external 6.4 KC signal.

The selection of which specific function to be performed by the low level logic must be simply programmed by the manner in which the modules are interconnected.

D. Inverter System Choice for Detail Study

The number of power switching components required in each inverter can be considered a valid point for choosing the type of inverter for further study. Based on the use of similar transistors for both the PAM inverter stages and the DC-DC converter bridge and the use of 20-amp power transistors in the PWM power inversion stages, a representative count can be determined. In the PAM inverter, thirty-two (32) switching devices are required. Twenty (20) 25-amp transistors in the power inversion stages,

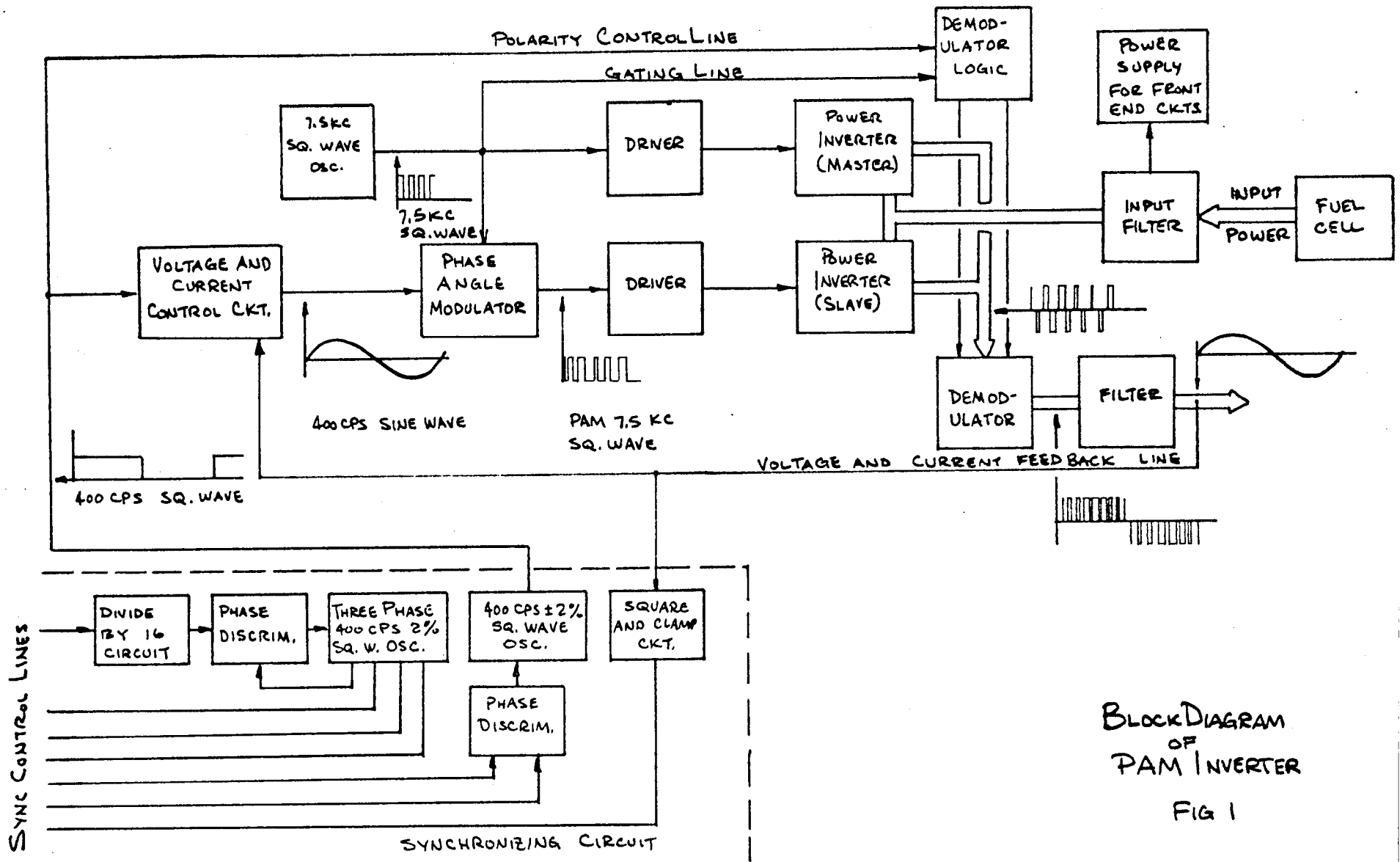
and twelve (12) gate turn-off SCR's in the demodulator. The rather large number of power semiconductors is required because the peak currents that must be switched by each device are a function of the peak load currents. No smoothing or averaging (energy storage) is performed which would lessen the peak currents.

The PWM inverter requires twelve switching devices (eight in the DC-DC converter and four in the PWM inversion stage). This characteristic gives the PWM inverter first consideration. The relatively small number of power transistors in the DC-DC converter is the result of filtering between the DC-DC converter and the PWM inverter bridge. The filtering averages the output power of the converter and smooths the current the power transistors must switch.

Another factor deserving consideration is audio noise generation. The PAM inverter uses power transformers which operate at 7.5 kilocycles nominally. In order to decrease the noise level produced by the transformers, the flux level must be reduced. If the flux level is reduced, however, the transformer weight increases which is unacceptabel. Increasing the operating frequency to above audible ranges is also unacceptable because the gate turn-off SCR's in the demodulator are frequency-limited to operation at 7.5 kilocycles. The PWM inverter has only one power transformer which is in the DC-DC converter. This transformer operates at 20 kilocycles which is above the normal audible range and therefore, is an essentially quiet inverter.

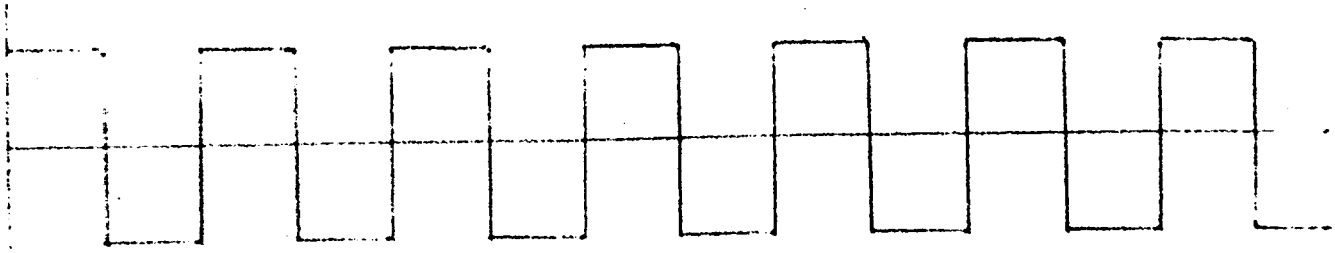
Complexity is also another important consideration. The PWM inverter is basically much simpler than the PAM inverter because of the fewer logical functions required by the control system. The area of the demodulator logic is not required by the PWM inverter.

Based on the above considerations, the inverter design which had been pursued was the PWM inverter.

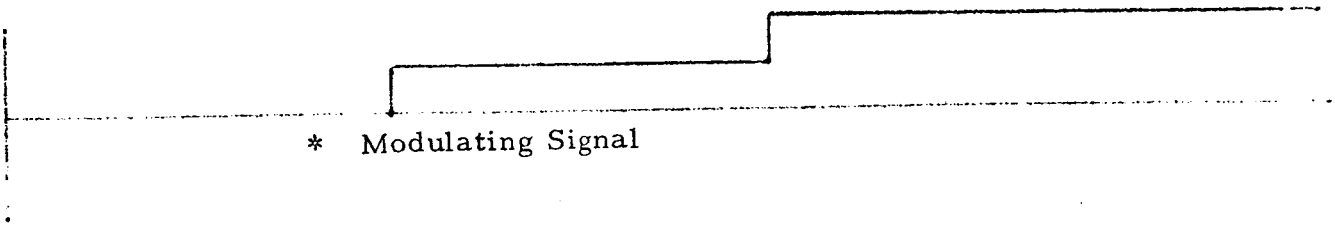


BLOCK DIAGRAM OF PAM INVERTER

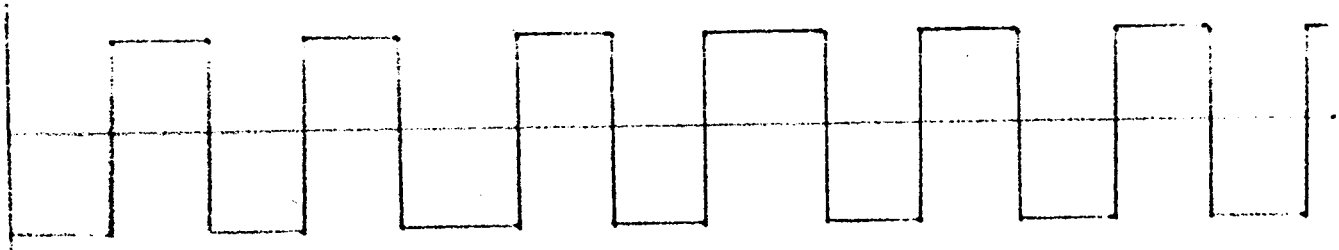
FIG 1



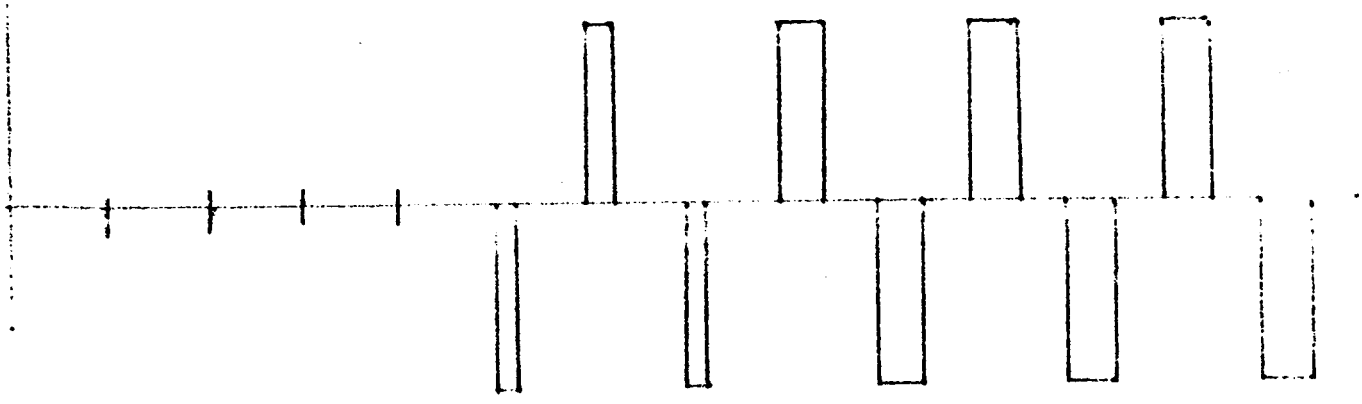
Unmodulated Inverter Output (Master)



* Modulating Signal



Phase Angle Modulated Inverter Output (Slave)

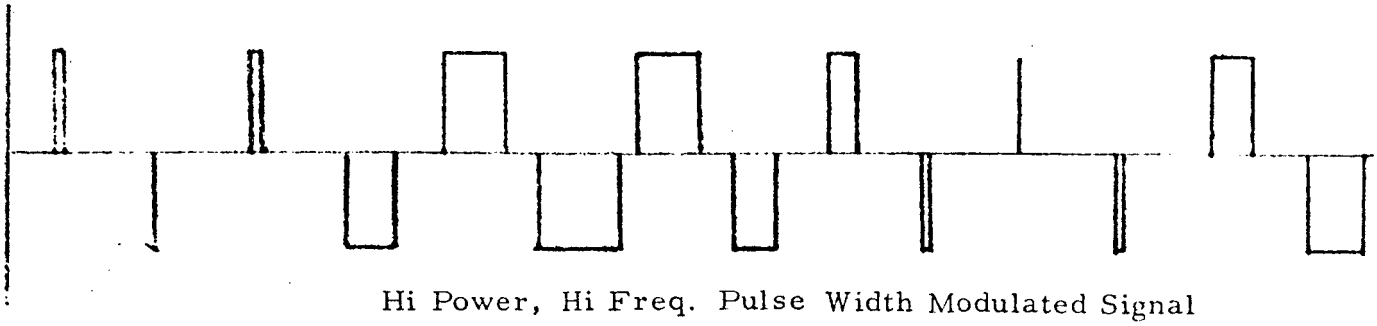


Summed Inverter Outputs

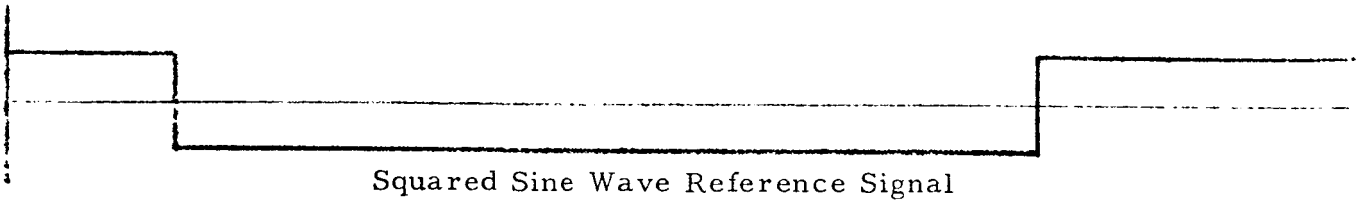
* Modulating Signal shown as voltage step for clarity purposes only.

PAM INVERTER WAVEFORMS

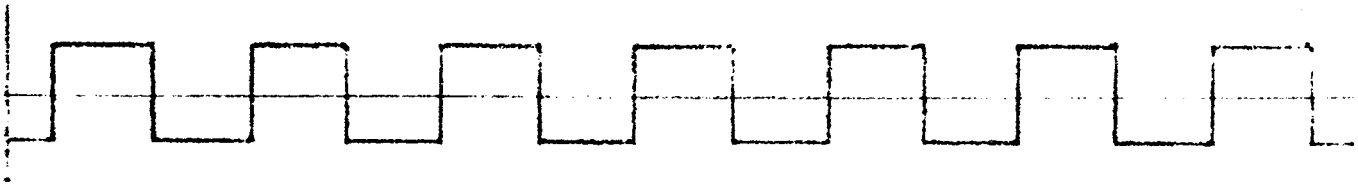
Fig 2



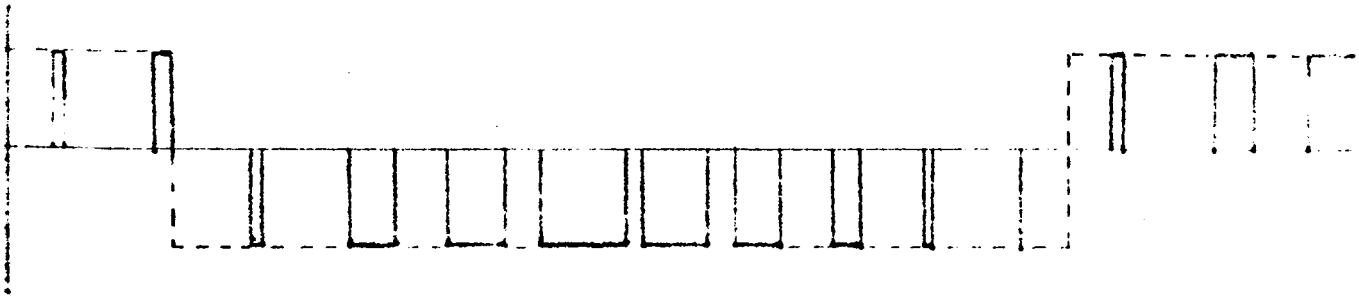
Hi Power, Hi Freq. Pulse Width Modulated Signal



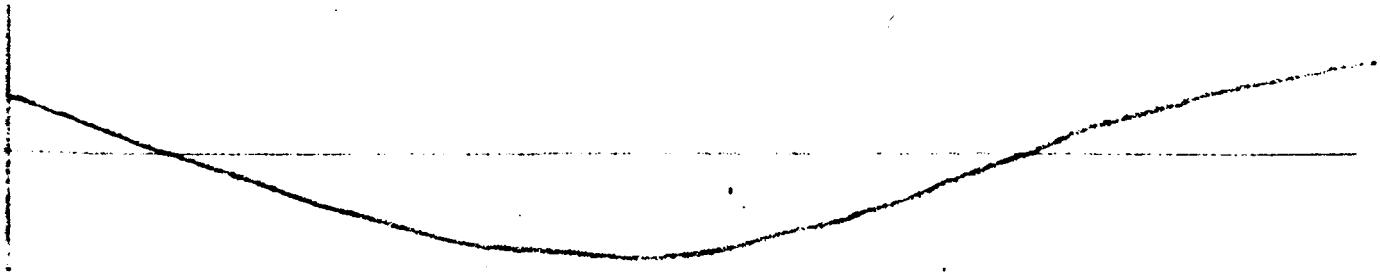
Squared Sine Wave Reference Signal
(A Demodulator Control Signal)



Hi Freq. Square Wave Oscillator Signal
(A Demodulator Control Signal)



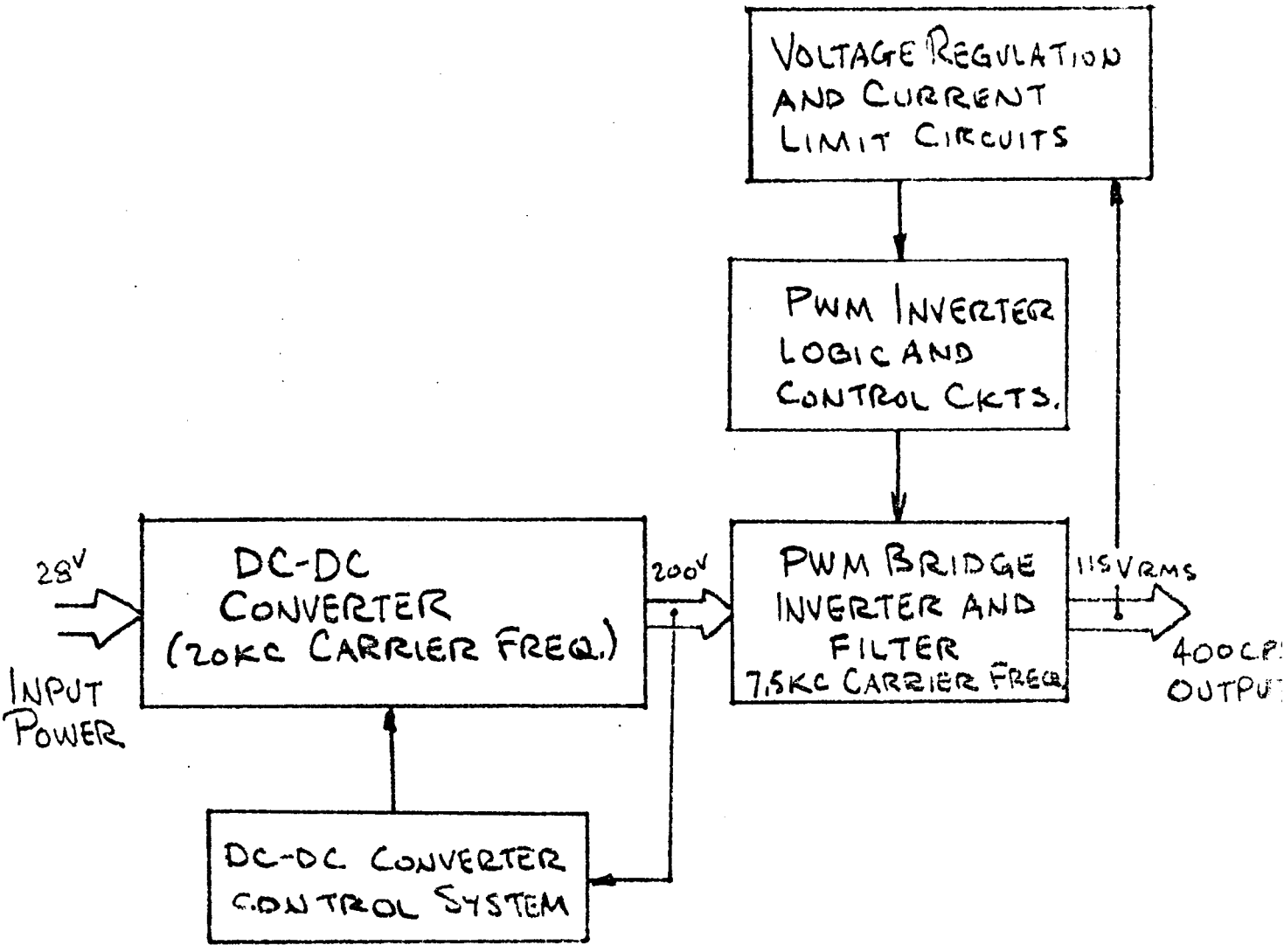
Demodulated Hi Power Waveform



Demodulator Waveforms

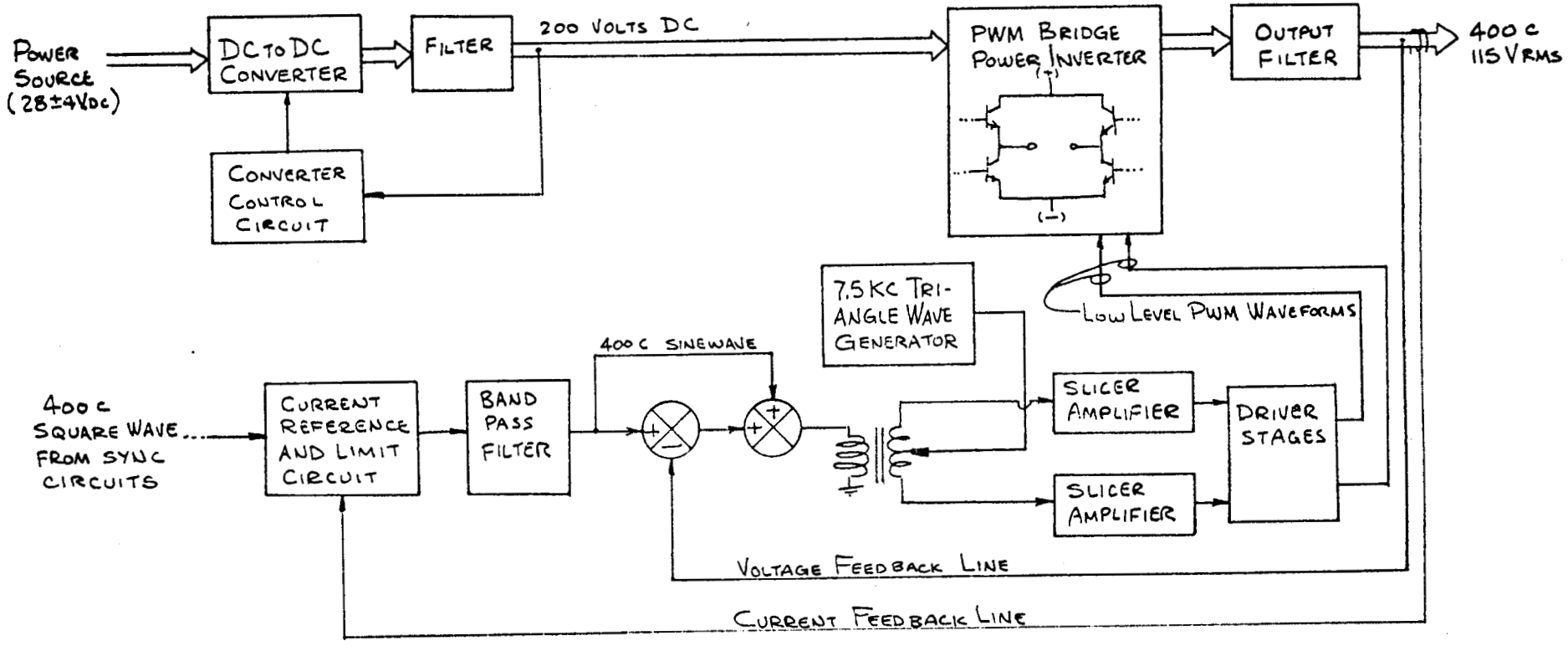
PAM INVERTER WAVEFORMS

Fig 3



PWM INVERTER
BLOCK DIAGRAM

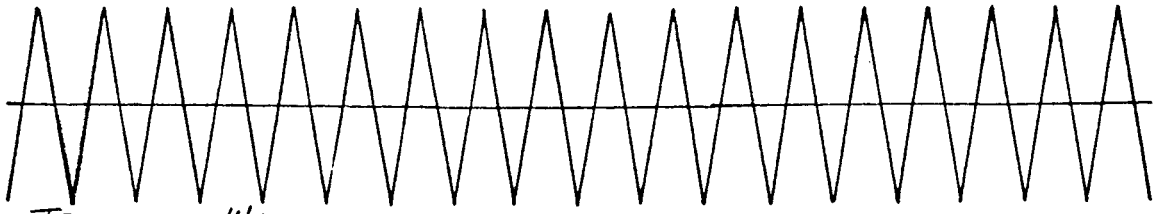
FIG. 4



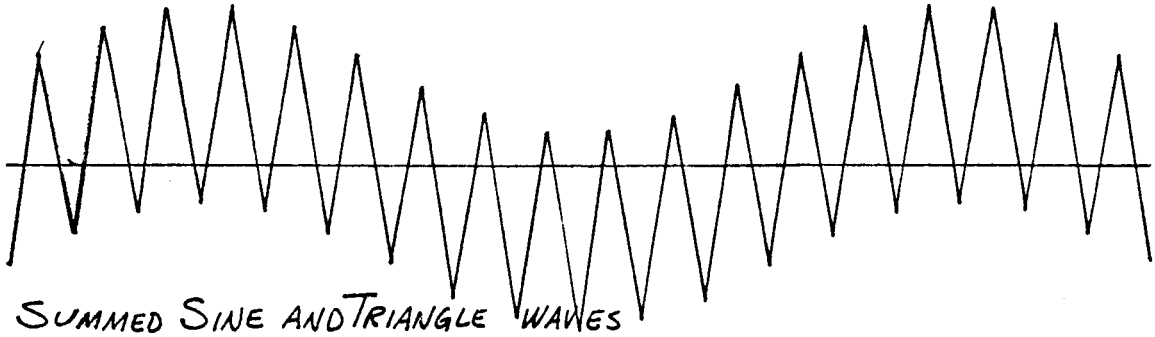
DETAILED PWM INVERTER BLOCK DIAGRAM

FIG. 5

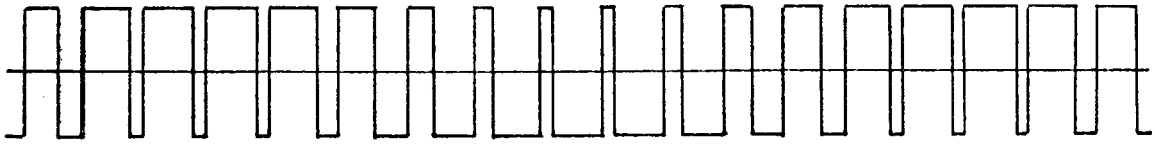
MODULATING SINE WAVE



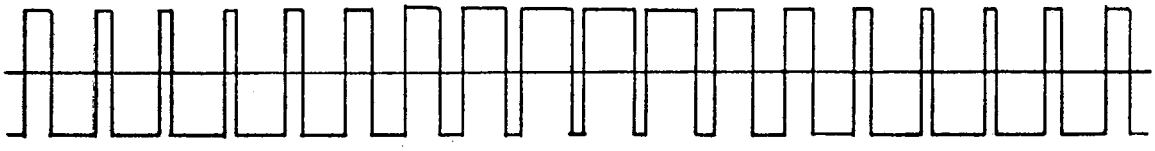
TRIANGLE WAVE



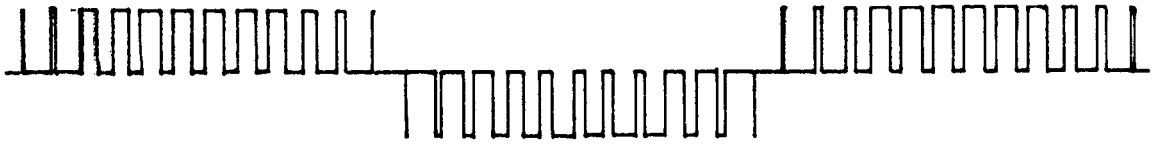
SUMMED SINE AND TRIANGLE WAVES



PULSE WIDTH MODULATED WAVE DERIVED FROM ABOVE WAVEFORM AFTER SLICING



COMPLEMENTARY PWM WAVEFORM



OUTPUT OF BRIDGE POWER INVERTER (UNFILTERED)

FILTERED OUTPUT VOLTAGE

PWM INVERTER WAVEFORMS
FIG 6.

III DETAIL DESCRIPTION OF THE PWM INVERTER

A. Power Source Impedance Considerations

In the design of a static inverter the interface between the power source and the inverter cannot be neglected. Under ideal conditions a power source will have perfect regulation and no internal transmission impedance. - this situation simplifies the inverter design because any fluctuation of input current to the inverter will not disturb the source bus. However - this is not the case with realistic power sources and distribution systems. Fluctuations of input current to the inverter cause ripple voltages to develop across the source impedances.

The specification for this inverter states that the ripple generated by the inverter onto the dc input line not exceed 0.5 volts peak. In the ideal case of a PWM inverter the internal energy storage is a minimum which means a nearly direct transmission of power from the source through the inverter to the load.

A simple mathematical analysis will reveal that the input current drawn by the inverter is an 800 cycle sine wave with a dc value. In some instances (leading or lagging loads) the input current is actually negative. The analysis is below.

V = rms output voltage
I = rms output current
P = power output
$v_o = \sqrt{2}\, V \sin(wt + a)$
$i_o = \sqrt{2}\, I \sin(wt + b)$
$p_o = v_o\, i_o$

The instantaneous power output is also

$$p_o = VI \cos(a-b) - VI \cos(2wt + a + b)$$

Since the PAM inverter contains a minimum of energy storage elements, the input power to the inverter can be expressed as the output power divided by the efficiency factor:

$$p_{in} = \frac{p_o}{n}$$

or

$$p_{in} = (V \text{ terminal})\,(i_1)$$

Assuming that the line and battery impedances are negligible, the current i_1 can be expressed as:

$$i_1 = \frac{p_{in}}{V \text{ terminal}}$$

however

$$p_{in} = \frac{p_o}{n}$$

therefore

$$i_1 = \frac{p_o}{(n)\ (V\ terminal)}$$

or

$$= \frac{V \cdot I \cdot \cos(a-b) - V \cdot I \cdot \cos\ (2\ wt + a + b)}{(n)\ (V\ terminal)}$$

The current i_1 is seen to consist of two components: the direct current component:

$$I_{dc} = \frac{V \cdot I \cdot \cos\ (a-b)}{n\ (V\ terminal)} \quad or \quad \frac{p_o}{n\ (V\ terminal)}$$

and an alternating component:

$$I_{AC} = \frac{-V \cdot I \cdot \cos\ (2\ wt + a + b)}{n\ (V\ terminal)}$$

or

$$I_{AC} = \frac{p_o\ \cos\ 2\ wt}{n\ (V\ terminal)}$$

The I_{AC} is the ripple current and occurs at twice the operating frequency of the inverter.

As the ripple current is impressed upon the line and battery impedances, an AC voltage is developed at the inverter terminals:

$$V_{AC} = I_{AC} \sqrt{(z_{Line})^2 + (z_{Battery})^2}$$

$$V_{AC} = (I_{AC})(Z_{Net})$$

where

$$Z_{Net} = \sqrt{(z_{Line})^2 + (z_{Battery})^2}$$

In order to eliminate the ripple voltage, V_{AC}, from appearing at the inverter terminals, the ripple current, I_{AC}, must be eliminated.

The method used to eliminate the ac current ripple is quite simple. In order to smooth a ripple current or voltage energy storage is required. The choice of where to insert energy storage devices is then a matter selecting the most economical point in the circuit in terms of weight and

efficiency. In this case the insertion of an 800 cycle LC trap across the dc input of the PWM power inverter bridge stage proved to be the best location. Figure 7 illustrates the location of trap and its function in block diagram form.

The 800 cycle trap effectively supplies a path for the 800 cycle AC component of current required by the PWM inverter. At the same time this trap causes only the DC component of current to be drawn from the converter - thereby smoothing the converter output current.

The other source of ripple current is the dc-dc converter. This ripple is caused by the high frequency switching mode of operation of the converter. A low value LC input filter eliminates this source of transient noise.

The sizes of the filter components in the inverter were derived from an analog computer simulation of the inverter. The complete inverter was simulated and the filter values adjusted under dynamic conditions of line and load until the required performance was obtained. The computer diagram is shown in appendix II.

B. Logic and Drive Circuits

1. INVERTER LOGIC AND CONTROL SYSTEM

A block diagram of the inverter control system is shown in figure 8. The diagram illustrates how a 400 cycle square wave from the synchronization circuits is used to control the frequency and phase of the inverter, how the pulse width modulation is accomplished, and how voltage regulation and current limiting is performed.

When the sync signal is absent the inverter free runs and is controlled by a UJT voltage controlled oscillator. The control voltage for the oscillator is derived from a phase detector which has an input from the inverter output and an input from the sync circuits - an absence of either signal causes the control output voltage of this circuit to disappear.

When a sync signal is present the phase detector develops a voltage which is proportional to the instantaneous phase difference of the inverter output and the sync signal. This control voltage then causes the voltage controlled oscillator to either speed up or slow down until exact synchronism is obtained. The maximum frequency excursion is limited by clamping diodes which prevents the oscillator from changing frequency more than a predetermined amount.

The square wave output of the oscillator is then clamped by a voltage controlled amplifier. The output of the amplifier is then shaped by a bandpass filter into a quality sine wave. Feedback to the voltage controlled amplifier holds the amplitude of the sine wave to a precise value determined by a zener diode. This precise sinewave is used as the voltage and waveshape reference for the inverter.

Current limiting is accomplished reducing the amplitude of the sinewave reference signal when the current exceeds a predetermined limit.

Voltage control is obtained by comparing the output voltage of the inverter with the sinewave reference signal. The difference between the two signals is an error voltage. This error voltage is then added to the sinewave signal to develop the modulation signal. The nearly instantaneous control of voltage and wave shape assures good transient wave form control of the inverter and eliminates the second harmonic distortion introduced into the system by the slight 800 cycle ripple present on the dc-dc converter output.

The PWM control waveforms are obtained by adding a 7.5 KC triangle wave to the modulating signals. The combined waves are then sliced to generate the low level PWM signals shown on figure 6.

Buffering of these signals by the driver circuits isolates the control system from the power inverter interface.

The circuit diagram shown in figure 9 and parts list reveals the use of many identical integrated circuits and components. (Parts list in table 1) The use of a basic integrated circuit operational amplifier for many uses such as summing networks, slicers, and buffers simplifies the control system also.

2. SYNCHRONIZATION CIRCUIT

The circuit diagram of the sync circuit is shown in Figure 8. The purpose of the sync circuit is to produce three 400 cps square waves displaced exactly 120 electrical degrees. The 400 cycle signals may or may not be synchronized by an external 6.4 KC signal. Also, in the event of the loss or extreme deviation in frequency of the external signal the sync system will automatically limit its output signal frequency.

The sync system consists of five major sections:

1. A divide by 16 circuit which develops a 400 cycle square wave from a 6.4 KC sync signal.

2. A phase detector circuit which produces a DC control signal which is proportional to the phase or frequency difference of its input signals.

3. A voltage controlled oscillator that produces a 2.4 KC pulse rate. This oscillator free runs at 2.4 KC ±1% or can be controlled by the phase detector output voltage.

4. A modulo-six binary coded counter. This counter produces three sets of complimentary signals which are used as inputs to a gating network. The counter is a self-correcting type with no ambiguous stable states.

5. Gating Network. This network gates the outputs of the modulo-six

counter into three 400 cycle square waves with an electrical phase displacement of exactly 120 degrees.

Integrated circuits are used as much as possible in this system. The parts list is shown in Table 2.

3. DC-DC CONVERTER CONTROL

The control for the dc-dc converter is shown in figure 11. It consists of two flip-flops, two dual nand gates, a 40 KC UJT oscillator, a pulse delay circuit, and a differential amplifier feedback-loop circuit.

The two flip-flops are triggered by UJT circuits - the first flip-flop is directly connected to the UJT oscillator and produces a 20 KC square wave which is used directly by the converter. The second flip-flop is triggered by a UJT pulse circuit which is gated by the dual nand gate circuits. The output pulse of UJT 2 is delayed by the RC charging circuit in its emitter circuit. The delay is inversely proportional to the RC circuit charging voltage.

The RC charging voltage is derived from the differential amplifier circuit which compared the converter output voltage to a zener diode reference voltage. As the output voltage exceeds the reference value the charging voltage decreases which causes a greater pulse delay. The delayed pulse triggers the second flip-flop later in time which produces a greater dwell time in the converter output. The greater dwell time then reduces the converter output voltage which reduces its deviation from the zener reference.

The parts list for the control is in Table 3.

C. Power Inverter

This bridge power inverter was designed using one 20-amp 325-volt transistor per leg. The schematic for this inverter is shown in Figure 13. The parts list for this inverter is Table 4.

The power transistor ratings permit the inverter at 500 VA steady-state, 750 VA overload, and 11.8 amps rms short circuit current. These ratings are exactly as required by the spec except for the 270 percent rated short circuit current. The spec requires 322 percent.

The lower parts count, light weight, and elimination of paralleled components make this inverter stage a most desirable configuration. In the event of the development of a 25-amp 325-volt transistor the short circuit current of 14-amp rms will be attainable.

An investigation was made for the application of positive current feedback as a means of supplying the required base drive current for the DC-DC converter and the DC-AC inverter power transistors. The positive current feedback scheme offers the following advantages over the more conventional fixed voltage drive scheme that is presently being proposed.

1. The storage and fall time of the power transistors will be essentially constant, independent of the collector current magnitude, because the base current is a function of the collector current. Therefore, the power transistors are never driven hard into saturation for low collector currents which would result in an increase in their storage and fall times.

2. The base drive circuit losses should be less, especially at the lower collector current level, thus improving the overall inverter efficiency.

3. The unequal load current sharing at turn-off caused by differences in storage and fall times of the parallel power transistors should be minimized using this scheme (as in the case of the DC-DC converter).

Circuits utilizing the current feedback base drive scheme were created for both the DC-DC converter used in the PWM approaches and the DC-AC PWM bridge inverter stages.

In figure 13 the current feedback drive transformers are described as T302, 303, 304, and 305. The emitter current for each power transistor must pass through the primary of the current transformer which induces a base drive current in the transistor which is proportional to the emitter current.

A turn-off coil is also on the current drive transformer to interrupt the drive current in the power transistor base. The pulse of current is derived from a saturating pulse transformer (SR 301 and 302) which triggers a transistor on.

The transistor conduction is initiated by a sustain drive transformer (T307, 308, 309, and 310). These transformers are driven by low power circuits which are designed to eliminate the problem of shoot-through.

Shoot-through is a condition which exists because of the finite storage time of the power transistors - the delay in turning off a transistor - say Q307 when Q308 is turning on causes a momentary short circuit across the high voltage dc bus.

A number of different circuit approaches were considered as a means of eliminating the momentary short-circuit conditions caused by the finite storage and fall times of the power transistors. A fixed time delay circuit

could be used to alternately delay the sustain drive turn-on for each half cycle. However, this circuit is not self-compensating. Therefore, its delay time must be made long enough to account for the increase in the power transistor storage and fall times caused by high junction temperatures, aging, and replacement with inherently slower transistors.

A self-compensating circuit utilizing either a current or a voltage sense circuit would account for these changes automatically. The load current sense circuit would require sufficient gain to operate satisfactorily under "no load" conditions to insure proper switching of the sustain drive circuits. Because of the difficulties in obtaining proper operation during "no load" conditions, the voltage sense circuit was used in the current feedback base drive scheme to eliminate the short-circuit problem since its operation is independent of the load current. The voltage snese circuit diverts the base current of the sustain drive transistor (say Q305) that should be turned "on" through the power transistor Q308 and blocking diode CR 307 until its storage and fall time has elapsed. During this time interval, transistor Q305 is prevented from being turned "on", hence preventing the turn-on of the power transistor Q307. Additional windings on the drive transformer provide a reverse bias voltage to the base-emitter junctions of the sustain transistors Q305, 306, 311, and 312 to insure that they will not be turned "on" during this "hold-off" time.

All the components used in the power inverter are specifically high speed types. The blocking diodes are fast recovery types. The zener diode spike clamps across each power transistor are sped up with the insertion of a high-speed rectifier in series with them.

D. DC-DC CONVERTER

The schematic diagram of the DC-DC converter is shown in Figure 14. The converter is a bridge-type system using two paralleled power transistors in each leg. Each power transistor is a 25 amp - 100 volt high speed device in a light-weight flat-package. It is an RCA type 2N3263 transistor.

Analysis of the converter/inverter interface revealed that between the overload and short circuit points of the inverter output VA characteristic the converter need only supply a maximum of 750 watts plus losses. Under short circuit conditions, the converter need only supply the losses to the inverter stage. Figure 15 will help explain this phenomena.

Figure 15 is a simplified diagram showing the major power switching and energy storage elements as they are connected in the inverter. The waveforms of the currents and voltages indicated on the diagram (Figure 15) are shown in Figure 16 - the waveforms are simplified slightly for clarity.

Under normal conditions of load from no-load to full-load the waveforms on Figure 16 apply to the diagram on Figure 15. Waveform C illustrates the instantaneous output power which is also proportional to the bridge inverter input power. Ignoring losses in the inverter, the instantaneous input power can be expressed as:

$$Po = (v_1)\ (i_1)$$

where $v_1 = (\sqrt{2})\ (V_1)\ \sin\ (wt)$

$i_1 = (\sqrt{2})\ (I_1)\ \sin\ (wt + \Theta)$

Θ = power factor angle

therefore

$$Po = V_1 I_1 \text{ Cos } (\Theta) - V_1 I_1 \text{ Cos } (2\ wt + \Theta)$$

also

$$Pin = Po \text{ (for discussion only)}$$

Dividing the input power Pin by the inverter stage input voltage (V_3) yields the inverter input current I_3. Since V_3 is a constant DC voltage, the current I_3 has a shape similar to the input power Pin and can be expressed as:

$$I_3 = \frac{V_1 I_1 \text{ Cos } (\Theta) - V_1 I_1 \text{ Cos } (2\ wt + \Theta)}{V_3}$$

The ac component of this current I_3 is $\frac{V_1 I_1 \text{ Cos } (2\ wt + \Theta)}{V_3}$ and is supplied by the LC trap of L 203 and C 203. This current is called I_4 on the diagram. The DC component of current or $\frac{V_1 I_1 \text{ Cos } \Theta}{V_3}$ is supplied by the converter and is called I_5 on the diagram. The trap then supplies AC current to the inverter and the converter supplies DC current which also satisfies the restriction that the converter can only deliver positive current to a load.

In the event of an overload or short circuit condition, the output voltage V_1 is reduced (to zero in the event of a short circuit).

The reduction of output voltage V_1 under overload conditions is controlled to limit the output VA to 750 maximum. Under a short circuit, the output

VA is zero since V_3 is zero.

When short circuited, the voltage V_2 is equal to the product I_1 and the reactance of L 301. The current I_3 is then:

$$I_3 = \frac{V_2 I_2 \text{ Cos } \Theta - V_2 I_2 \text{ Cos } (2 \text{ wt} + \Theta),}{V_3}$$

Under short circuit the power factor angle is 90° since the only load is L 301.

This condition causes the DC component of current to reduce to zero. The trap continues to deliver the AC current as before. In actual practice, a small DC current would exist because it must replace the losses caused by the flowing of the AC load current in the trap and output filter and the switching losses.

With the above considerations, the maximum current that the DC-DC converter transistors are required to switch can be determined.

The worst case operating conditions would be when the inverter is required to deliver a maximum overload of unity power factor when running from a low voltage bus. Under these conditions, the DC-DC converter transformer would be producing square waves of about .95 percent "on" time. The current delivered by this converter is:

$$I_5 = \frac{Po}{(V_3)\, n}$$

where

$Po = 750$ watts

$V_3 = 200$ volts

$n = .9$ (efficiency factor)

therefore

$$I_5 = \frac{750}{(200)\,(.9)} = 4.17 \text{ amps}$$

The turns ratio of the transformer is about 10:1 which causes the transistor current to be about 41.7 amp maximum. A small factor about 0.1 can be added to this current for transformer magnetizing current and efficiency considerations. This brings the transistor current to 45, 8 amps which can be readily handled by two twenty-five amp transistors connected in parallel as shown in Figure 14.

The power transistors in the converter are driven by a positive current feedback scheme which limits drive losses considerably as compared to a voltage drive system. Also, in the event of a very low input voltage, the base-drive current path is opened by means of a transistor which is normally turned on, this technique is required to prevent latch-up of the transistors in the event insufficient turn-off current is available due to low input voltage.

The same technique to prevent momentary short circuits during turnoff of the transistors used in the PWM inverter stage is used in the converter. The power transformer for the converter is a specially designed type utilizing a ferrite cup-core. The combination of the ferrite core and the use of a very high operating frequency (20 KC) permits the converter to operate quite efficiently and silently. The quietness of operation is certain because transformer vibrations would be above the audible range.

The capacitors used in the filters of the converter (and inverter) are of the high efficiency Polycarbonate type. The high efficiency of these capacitors is also complimented by their relatively low weight when compared to identical value capacitors having a paper dielectric.

Separate balancing reactors are used for steady-state load current sharing. The balancing reactor function can be included as part of the current feedback transformers with a possible weight savings.

E. LOGIC AND DRIVE POWER SUPPLY

The purpose of the power supply is to generate bias voltages for the logic drive functions of the inverter and the isolated voltages required by the sustain drive transistors in both the converter and inverter. The bias voltages generated by the power supply are regulated by a nearly lossless method of phase shifting two square inverters and summing the secondary coils of the output transformers.

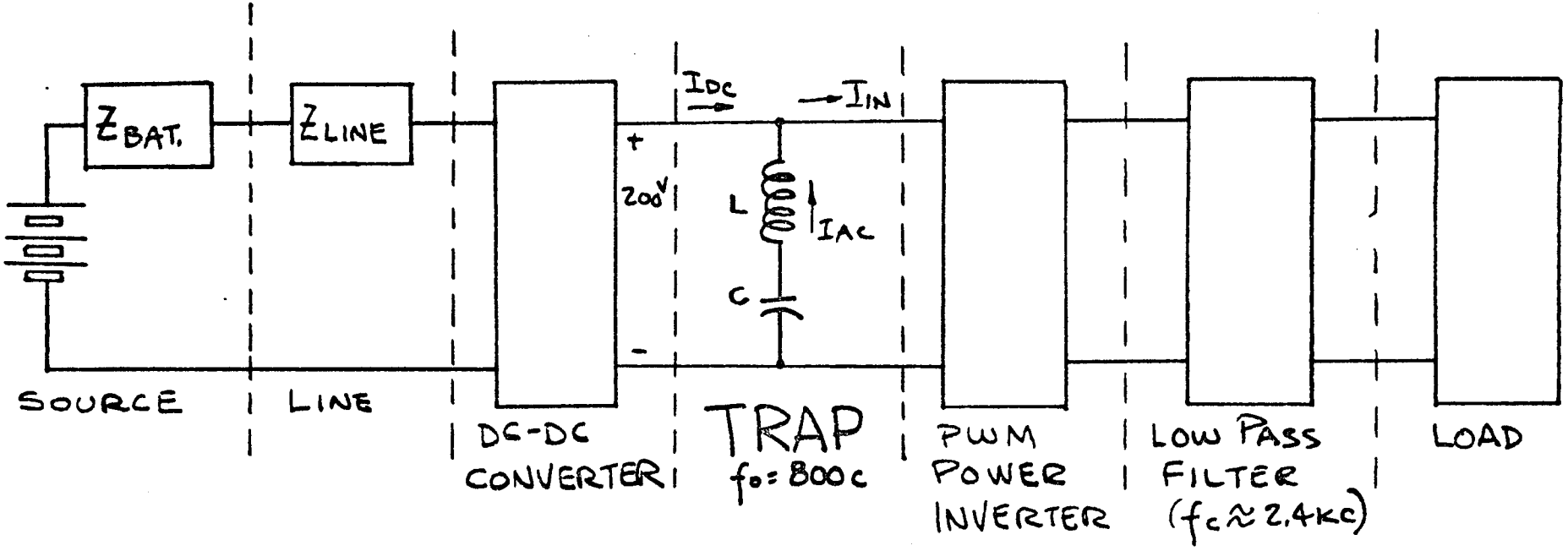
The block diagram of the power supply is shown in Figure 17. A ten kilocycle unijunction oscillator generates pulses which trigger a flip-flop called the master. The flip-flop develops five kilocycle square waves which drive a square wave power inverter and a gating network. A second flip-flop, called the slave, also drives a power inverter. This flip-flop is driven by an adjustable delay circuit.

The adjustable delay circuit is a gated unijunction pulse generator. The pulse delay is inversely proportional to the control input current. The slave flip-flop is connected to the second square wave power inverter in a manner which causes the two square wave power inverters to become more out of phase as the control input increases.

The control and reference circuit is a two input circuit. The basic circuit is a current generator that produces a charging current for the timing capacitor in the delay circuit. The charging current is proportional to the inverter supply voltage which forms the first control loop. The higher the supply voltage is the larger the charging current gets. The larger charging current causes the delay circuit to produce shorter delays.

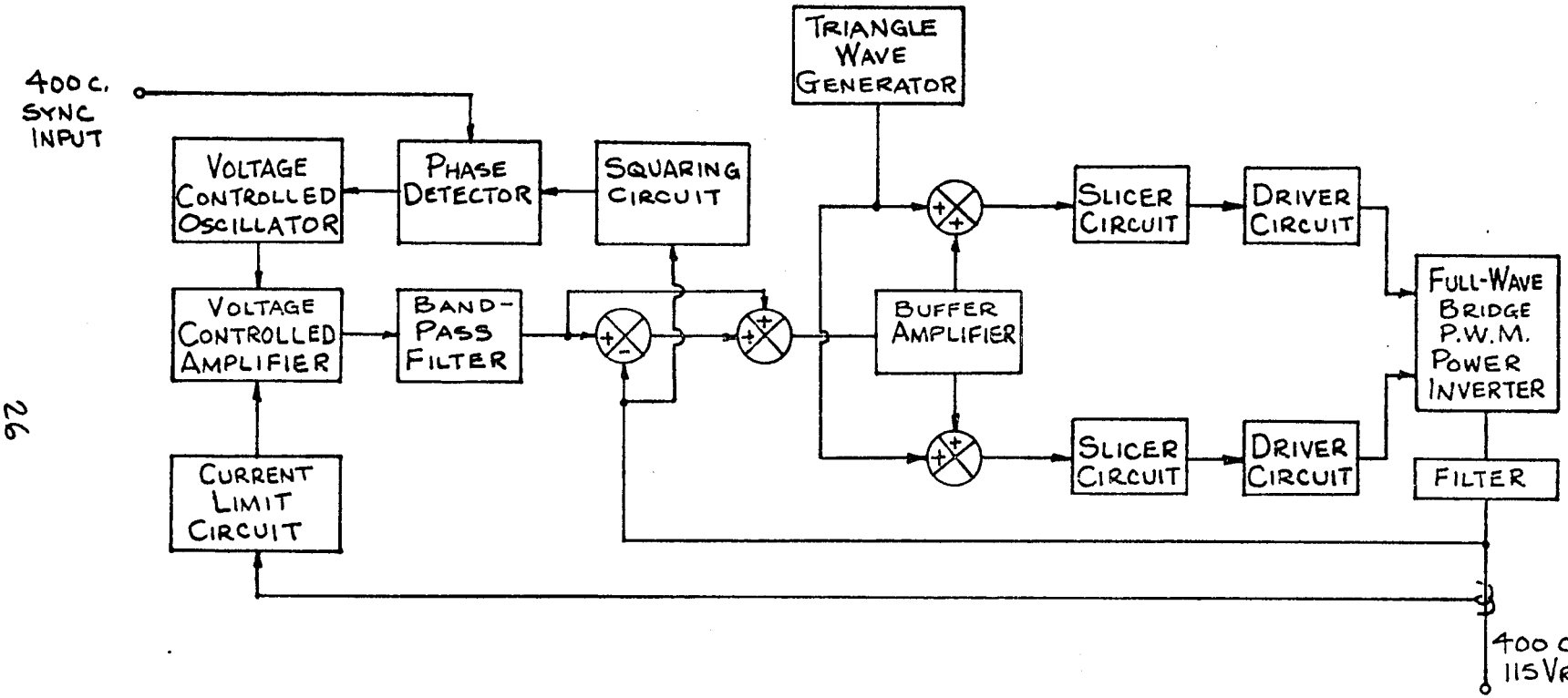
A secondary control loop is an auxiliary input to the current generator. The auxiliary input causes the generator to generate more current as the output voltage of the power supply exceeds a zener diode reference. This secondary loop is of low gain and therefore high stability. The low gain is satisfactory because this loop is required only for trimming the power supply output voltage.

The schematics for the power supply are shown in Figure 18 and 19 and the parts lists is in Table 6. The schematic diagram shows a set of cross coupling diodes (CR 606, 607, and CR 614, 615). These diodes are used to eliminate the shoot-through problem caused by storage time in the power transistors.



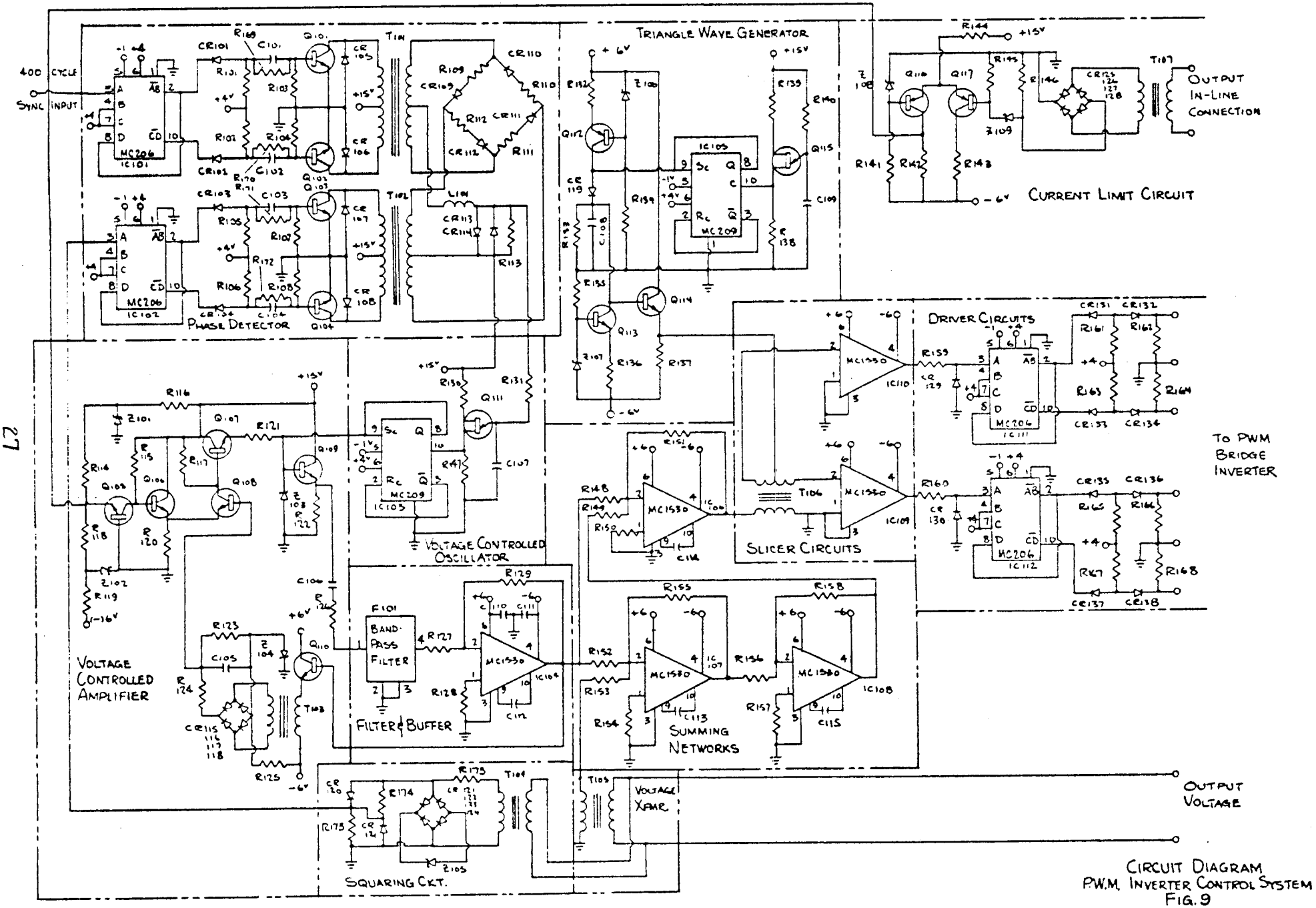
BLOCK DIAGRAM
ILLUSTRATING THE 800 CYCLE TRAP

FIG. 7

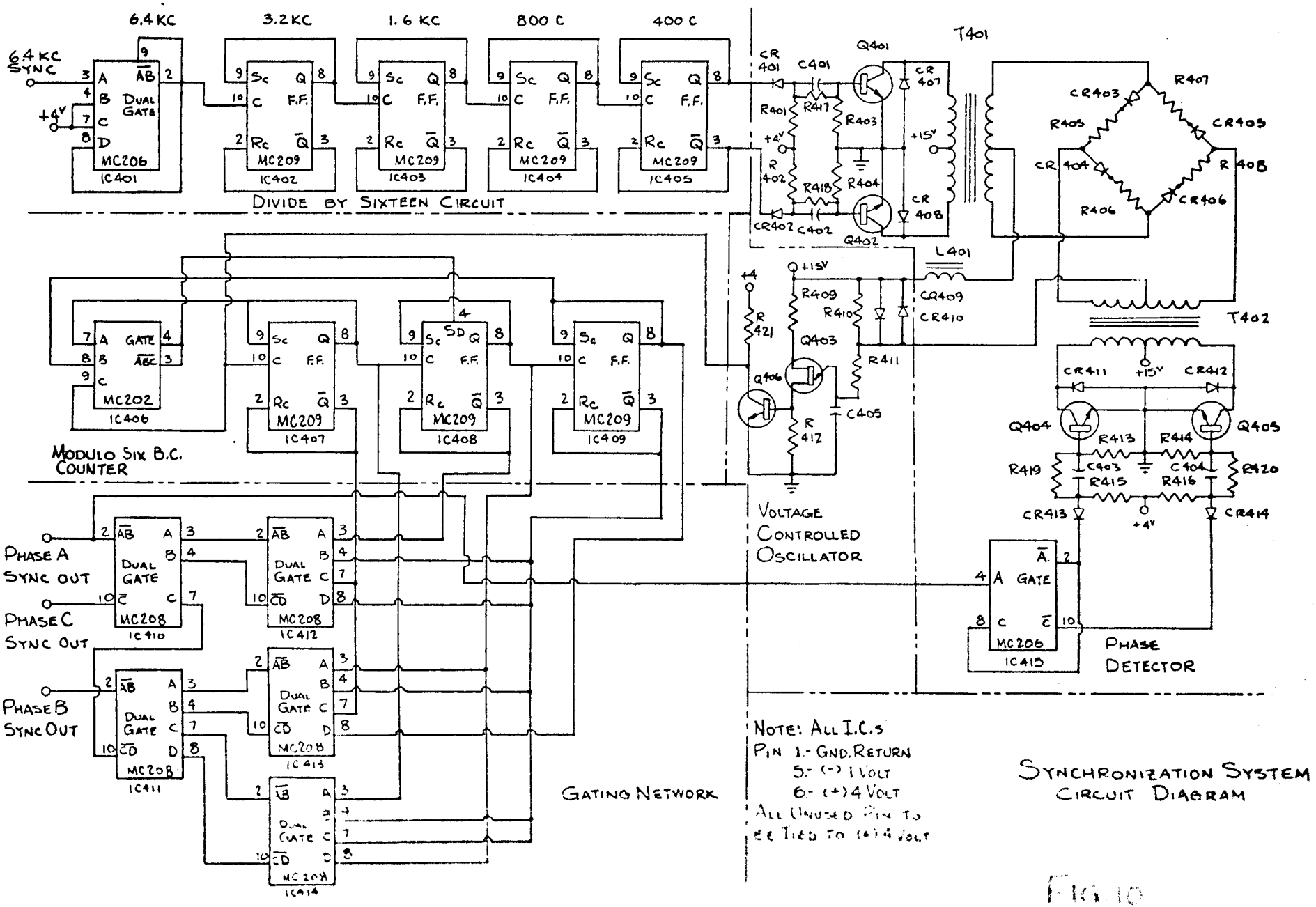


BLOCK DIAGRAM
PWM INVERTER CONTROL SYSTEM

FIG. 8



CIRCUIT DIAGRAM
P.W.M. INVERTER CONTROL SYSTEM
FIG. 9



SYNCHRONIZATION SYSTEM
CIRCUIT DIAGRAM

Fig 10

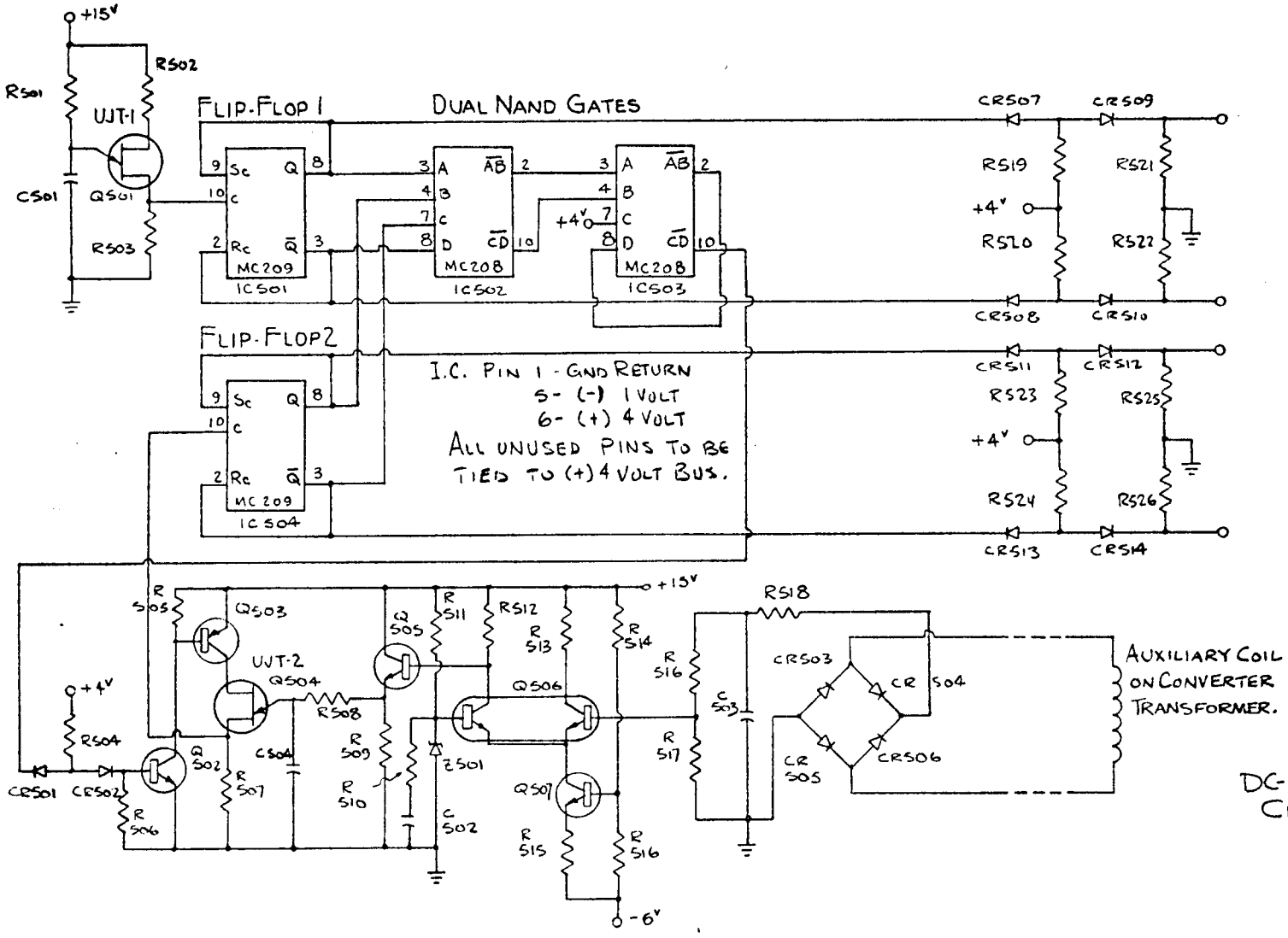
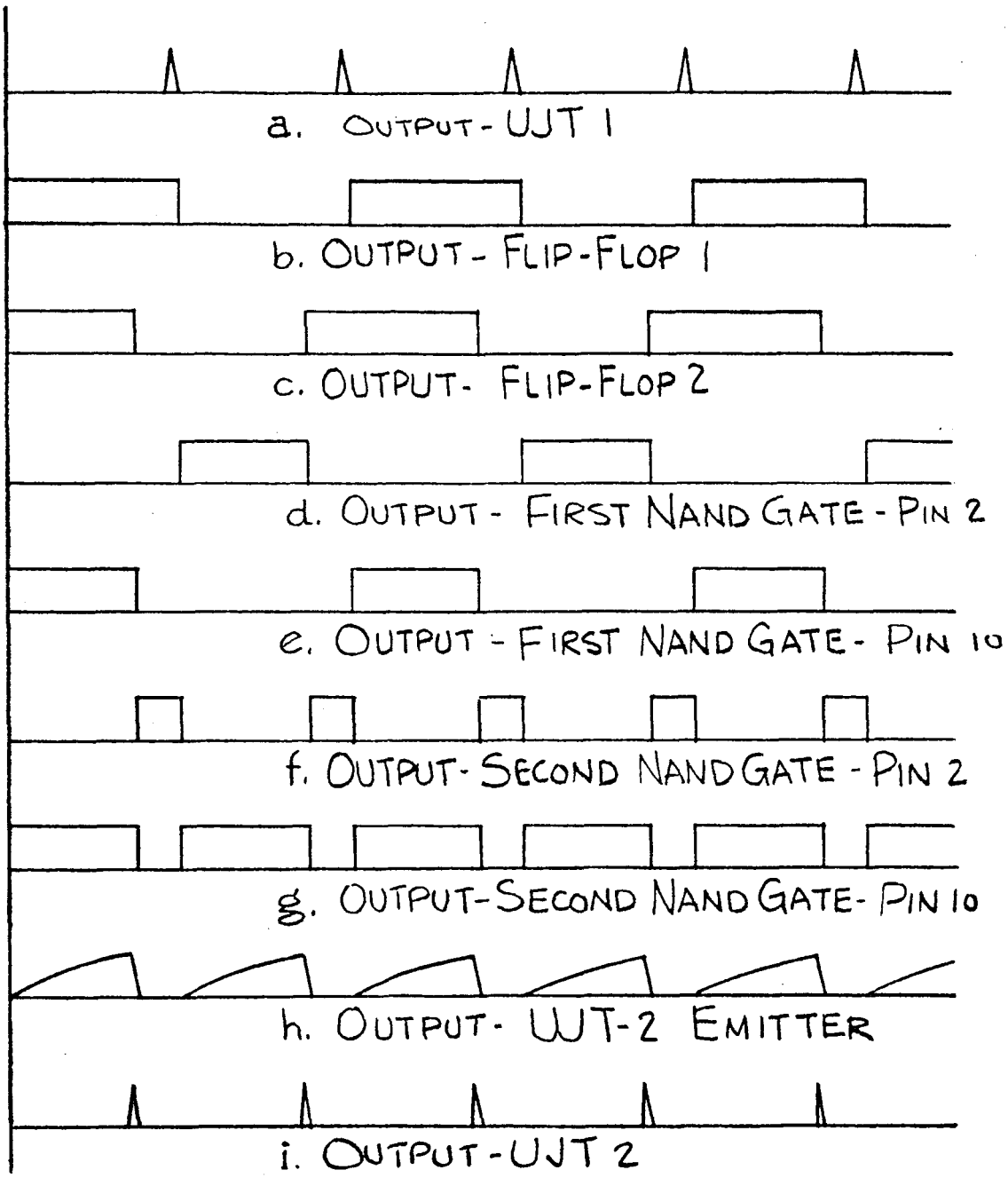
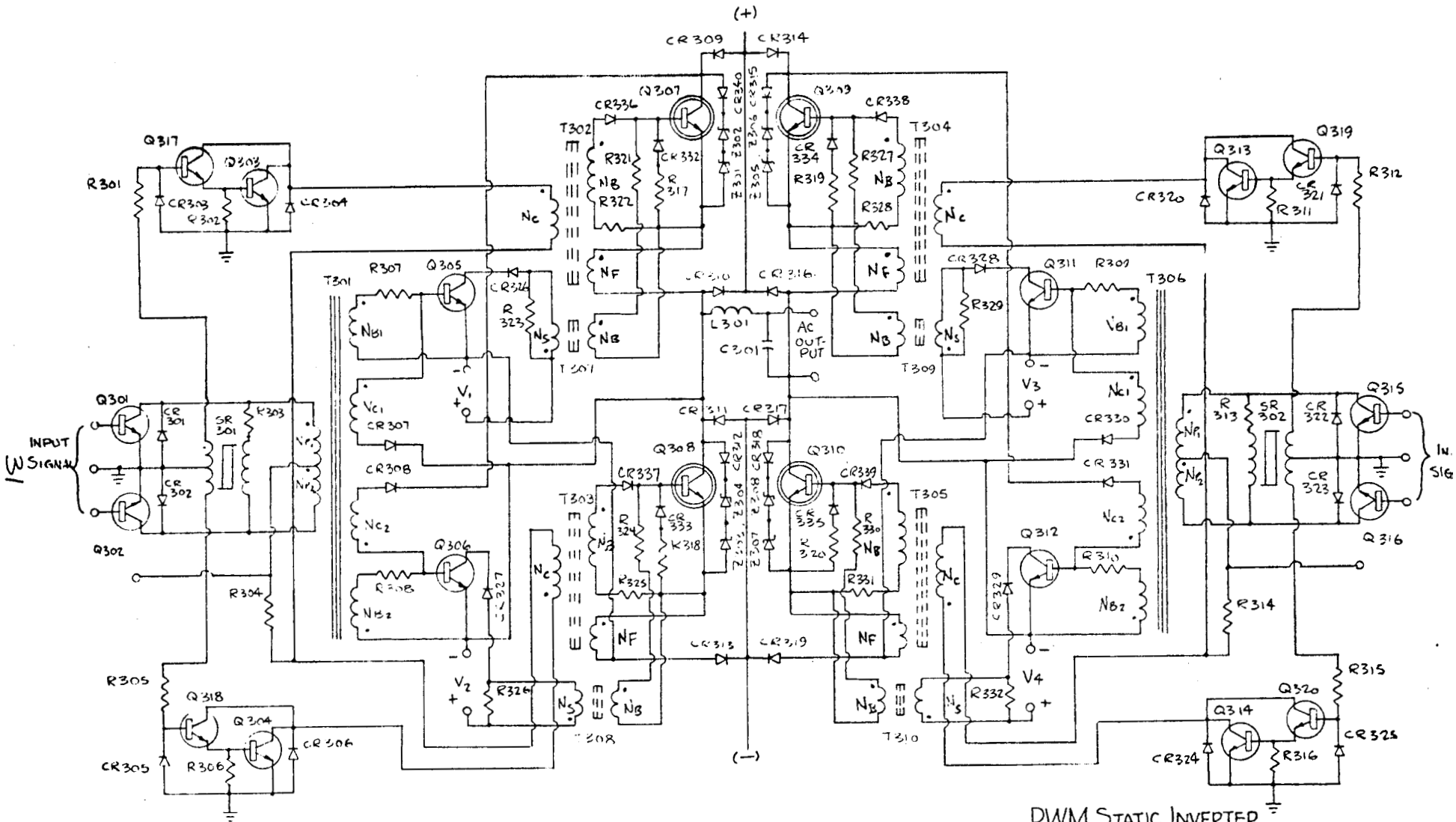

+15V
RS01
RS02
UJT-1
CS01
QS01
RS03
FLIP-FLOP 1
DUAL NAND GATES
MC209
IC S01
MC208
IC S02
IC S03
+4V
FLIP-FLOP 2
IC S04
I.C. PIN 1 - GND RETURN
5- (-) 1 VOLT
6- (+) 4 VOLT
ALL UNUSED PINS TO BE TIED TO (+) 4 VOLT BUS.
CRS07
CRS09
RS19
RS21
RS20
RS22
CRS08
CRS10
CRS11
CRS12
RS23
RS25
RS24
RS26
CRS13
CRS14
DRIVE SIGNALS TO DC-DC CONVERTER.
QS03
UJT-2
QS04
QS05
QS06
QS07
QS02
RS18
CRS03
CR S04
CRS06
CR S05
C S03
AUXILIARY COIL ON CONVERTER TRANSFORMER.
CRS01
CRS02
Z S01
C S02
-6V
DC-DC CONVERTER CONTROL CIRCUIT DIAGRAM

FIG. 11



DC-DC CONVERTER CONTROL WAVEFORMS

FIG. 12



PWM STATIC INVERTER
POWER OUTPUT STAGE
FIG. 13

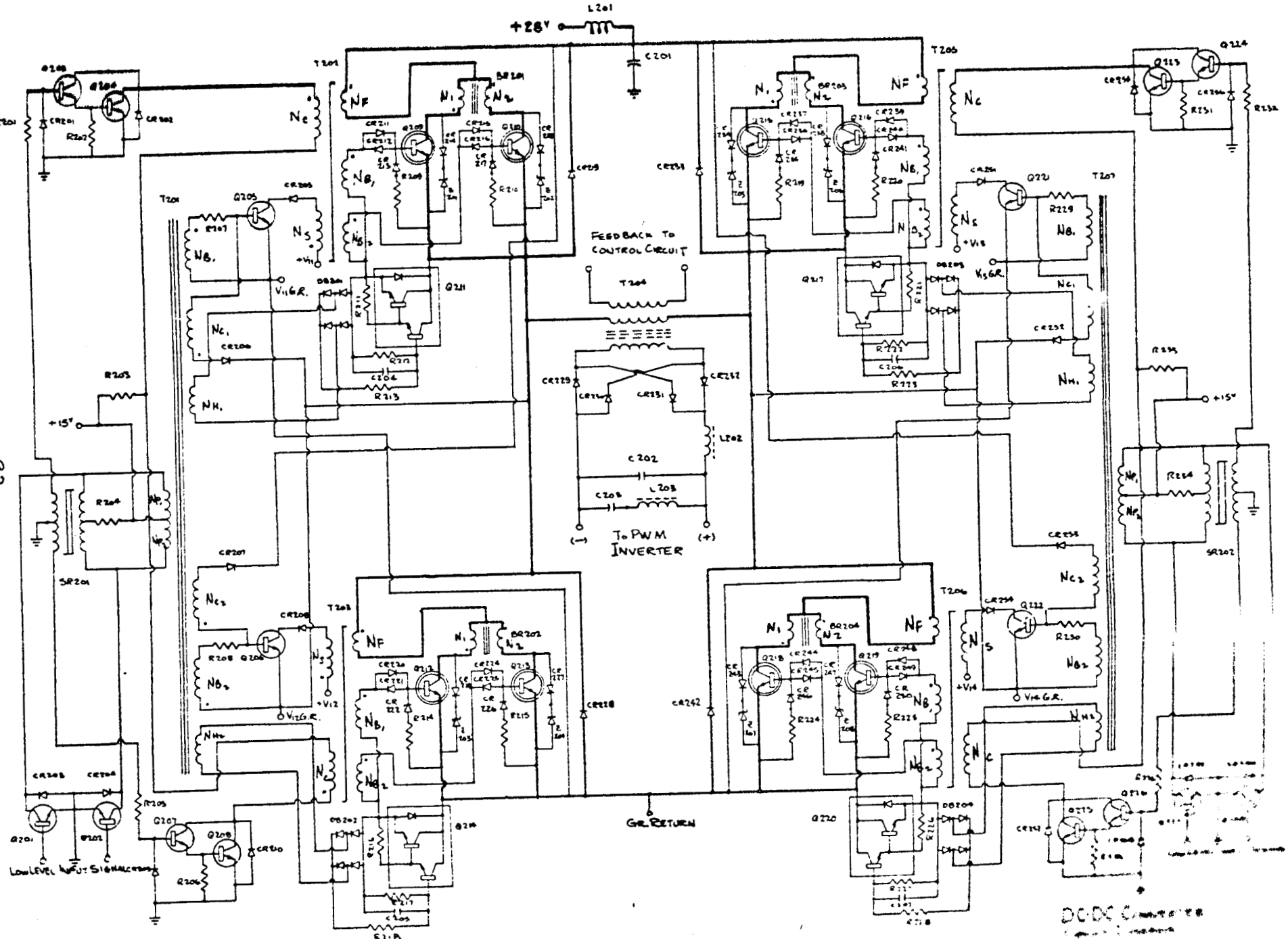
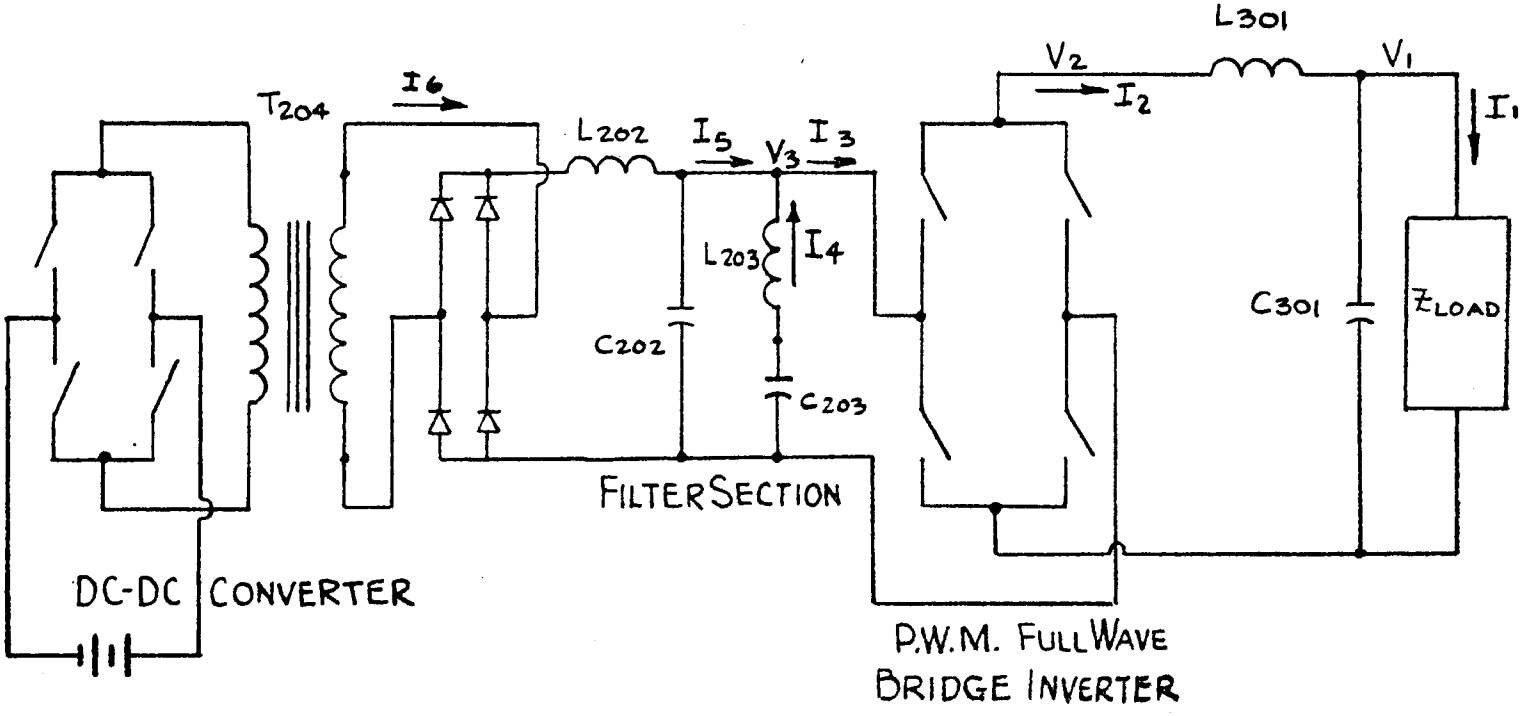
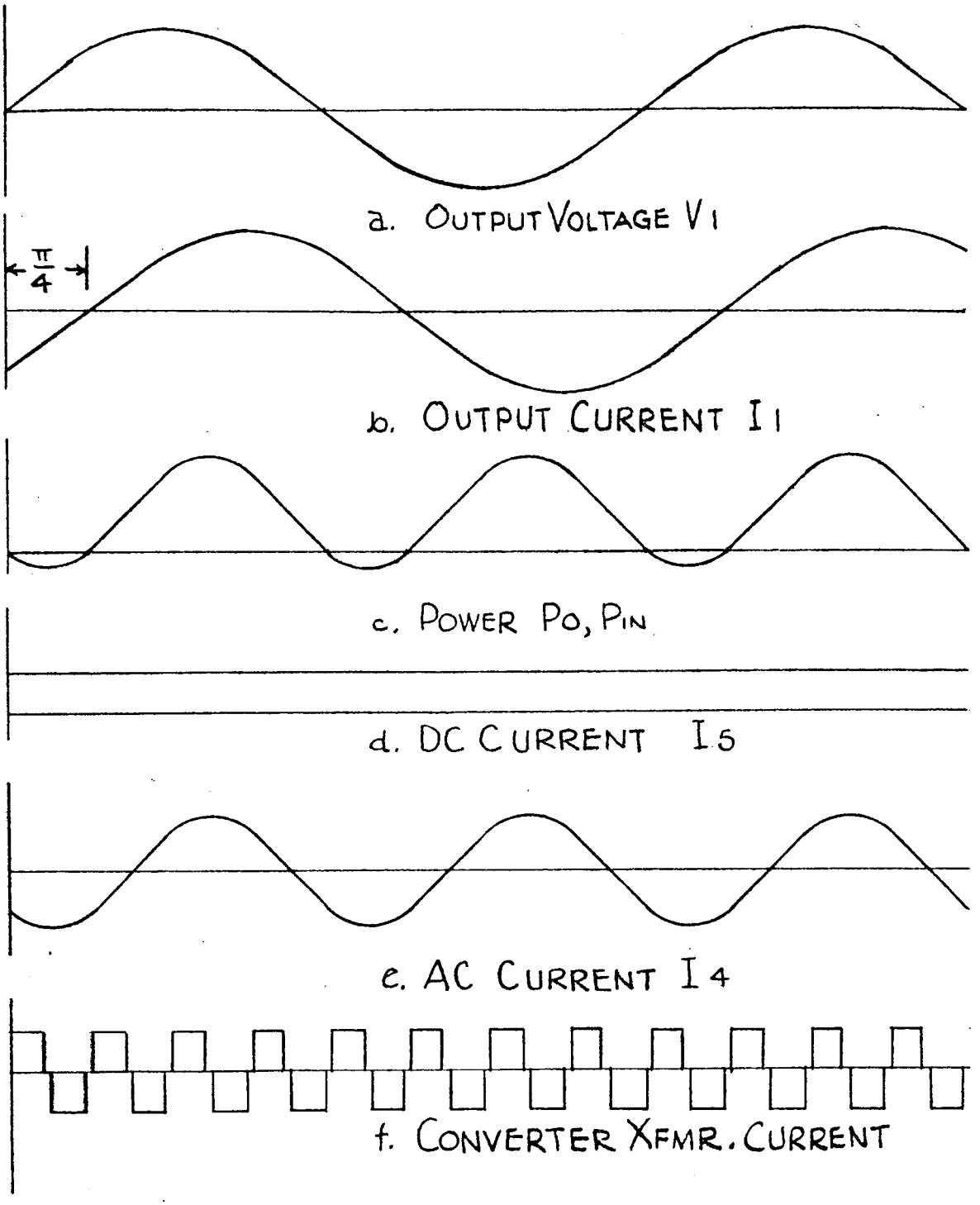

+28V
L201
C201
T201
T202
T203
T204
T205
T206
T207
Q201
Q202
Q203
Q204
Q205
Q206
Q207
Q208
Q209
Q210
Q211
Q212
Q213
Q214
Q215
Q216
Q217
Q218
Q219
Q220
Q221
Q222
Q223
Q224
FEEDBACK TO CONTROL CIRCUIT
TO PWM INVERTER
(−)
(+)
L202
C202
C203
L203
SR201
SR202
SR203
SR204
GR. RETURN
+15V
+V12
+V14
+V15
LOW LEVEL INPUT SIGNALS
DC/DC Converter

FIG. 14



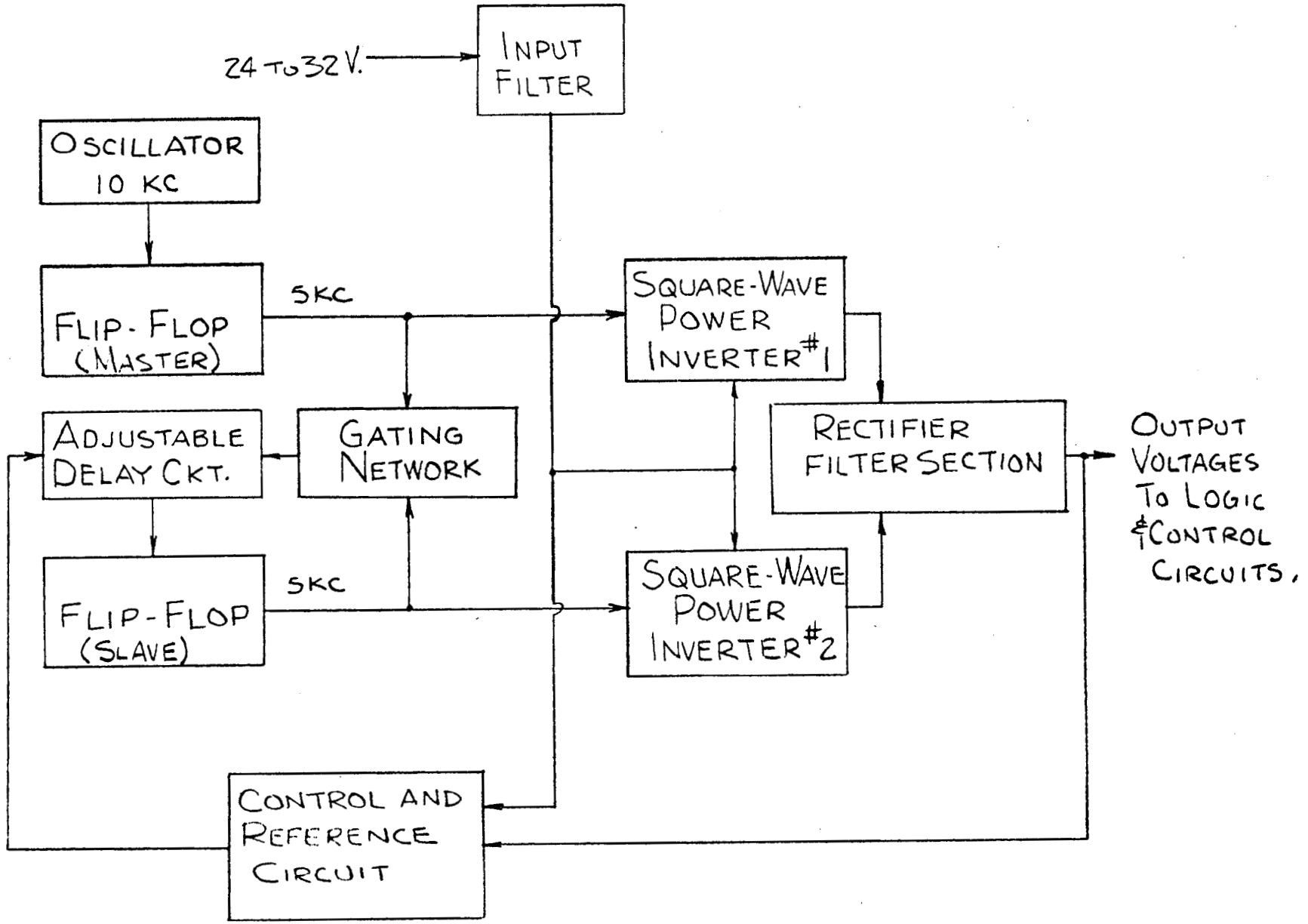
SIMPLIFIED DIAGRAM - P.W.M. STATIC INVERTER

FIG. 15



WAVEFORMS-P.W.M. STATIC INVERTER

FIG 16



BLOCK DIAGRAM
LOGIC & DRIVE POWER SUPPLY
FIGURE 17

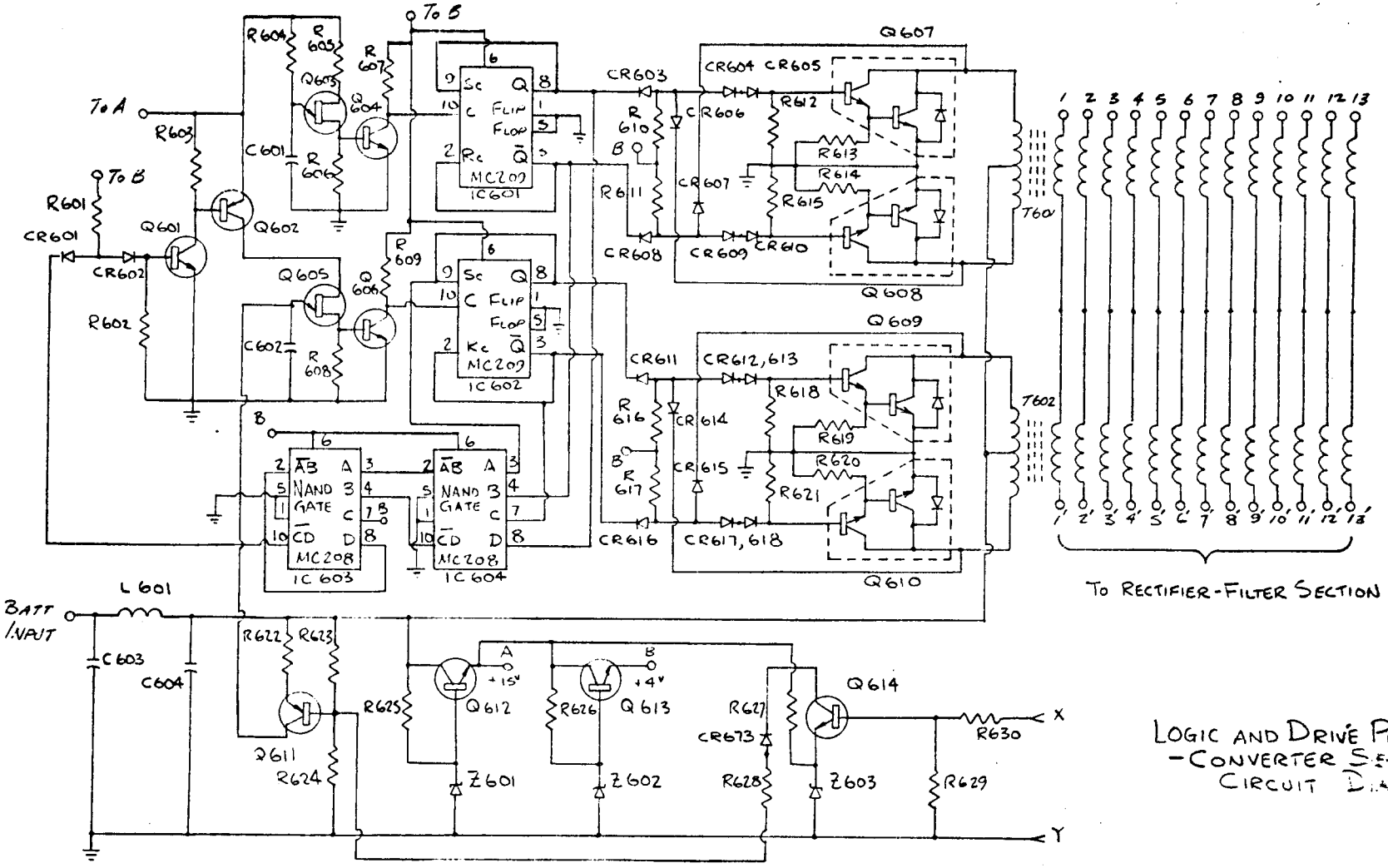
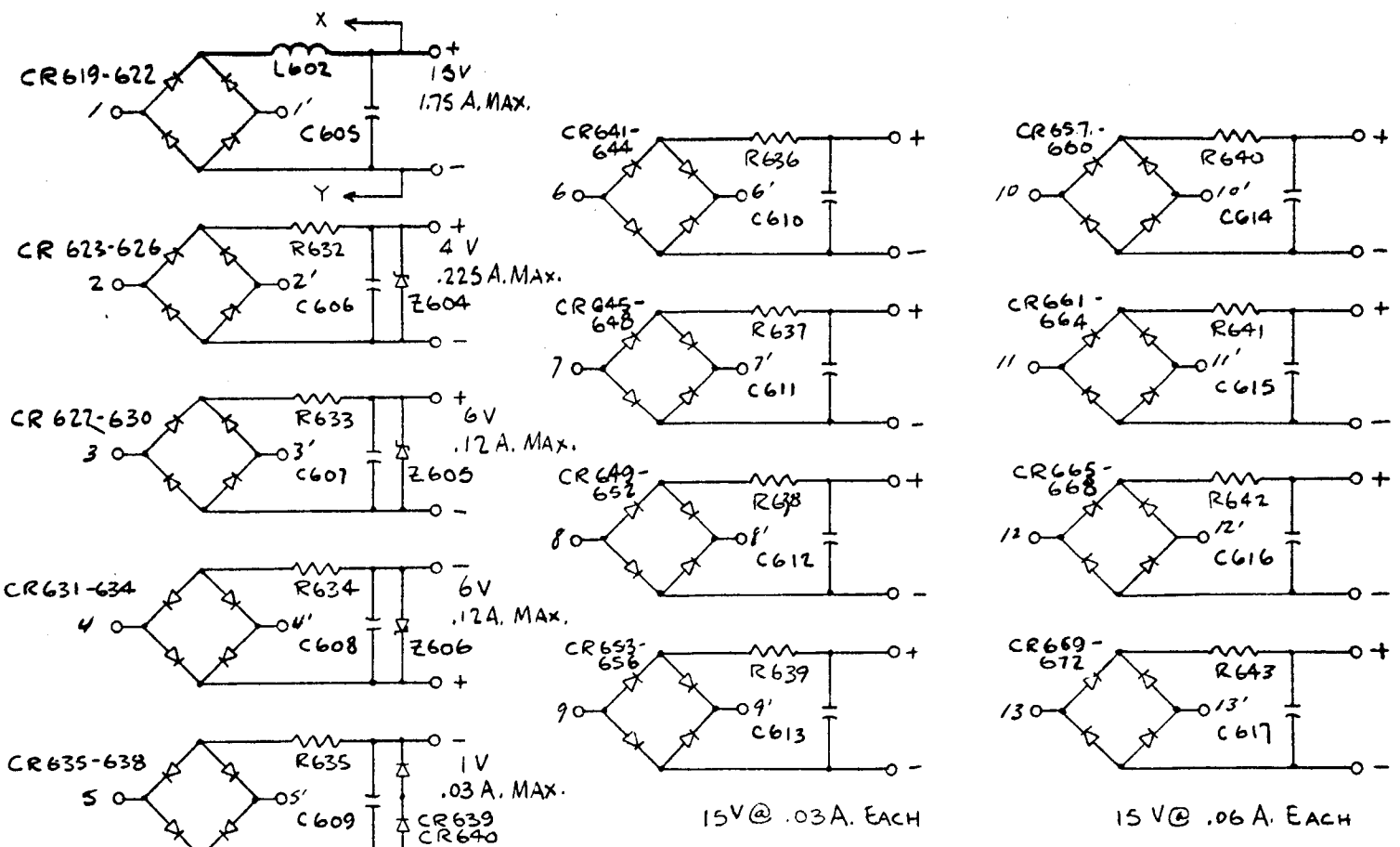


Figure 18

Logic and Drive Power Supply
-Converter Section
Circuit Diagram



LOGIC AND DRIVE POWER SUPPLY
-RECTIFIER AND FILTER SECTION-
CIRCUIT DIAGRAM

FIGURE 19

TABLE 1
PARTS LIST - INVERTER CONTROL SYSTEM

Item No.	Description	Circuit Designation	Quan.
1.	2N2222 transistor by Motorola NPN Silicon	Q101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 113, 114.	12
2.	2N2904 transistor by Motorola PNP Silicon	Q112, 116, 117	3
3.	2N491B Unijunction transistor by G.E.	Q111, 115	2
4.	MC206F Dual nand gate by Motorola	1C101, 102, 111, 112	4
5.	MC209F Flip-Flop by Motorola	1C103, 105	2
6.	MC1530F Operational Amplifier by Motorola.	1C104, 106, 107, 108, 109, 110	6
7.	1N914B Silicon diode	CR 101 thru 138	38
8.	1N748A Silicon zener diode	Z102, 105, 106, 107, 108.	5
9.	1N751A Silicon zener diode	Z101, 103, 104, 109	4
10.	DOT-25 transformer by UTC	T101, 102	2
11.	DOT-21 transformer by UTC	T106	1
12.	DOT-19 transformer by UTC	T 103	1
13.	Series 535 - 1.0 watt, 400 cycle transformer by Arnold Magnetics Co.	T 105	1

TABLE 1
PARTS LIST - INVERTER CONTROL SYSTEM (cont'd.)

Item No.	Description	Circuit Designation	Quan.
14.	Series 535 - 1.0 watt 400 cycle transformer by Arnold Magnetics Co. Part No. 535-767.	T 104	1
15.	Current transformer TRW Part No. 306222	T 107	1
16.	Resistor - 4.7K - 1/4 watt - 5%	R101, 102, 105, 106, 159, 160, 161, 163, 165, 167	10
17.	Resistor - 1.0K - 1/4 watt - 5%	R113, 169, 170, 171, 172, 115.	6
18.	Resistor - 1.5K - 1/4 watt - 5%	R103, 104, 107, 108, 162, 164, 166, 168.	8
19.	Resistor - 1.2K - 1/4 watt - 5%	R109, 110, 111, 112	4
20.	Resistor - 2.7K - 1/2 watt - 5%	R117	1
21.	Resistor 2.0K - 1/2 watt - 5%	R118, 144	2
22.	Resistor 1.0K - 1/2 watt - 1%	R116, 114, 121, 123, 124, 142, 143.	7
23.	Resistor - 220 ohm 1/2 w - 5%	R119, 120, 125, 134, 135, 141, 146.	7
24.	Resistor - 470 ohm 1/2w - 5%	R122, 173, 174, 175, 130, 137, 139.	8
25.	Resistor - 10K - 1/2w 1%	R126, 127, 129, 152, 153, 155, 151, 148, 149, 156, 158.	11

TABLE 1
PARTS LIST - INVERTER CONTROL SYSTEM (cont'd.)

Item No.	Description	Circuit Designation	Quan.
26.	Resistor 3.3K - 1/2w - 1%	R150, 154	2
27.	Resistor 4.7K - 1/2w - 1%	R128, 157	2
28.	Resistor - 2.74K-1/2w-1%	R132	1
29.	Resistor - 5.48K-1/2w-1%	R136	1
30.	Resistor - 50K-1/4w - 5%	R 131, 133	2
31.	Resistor - 47 ohm-1/2w 5%	R147, 138	2
32.	Resistor - 6.8K - 1/2w-1%	R140	1
33.	Resistor 10K - 1/2w - 5%	R145	1
34.	Capacitor - 0.5 microfarad 50 volt polycarbonate film type.	C101, 102, 103, 104	4
35.	Capacitor-0.1 microfarad 50 volt polycarbonate film type.	C110 through 115	6
36.	Capacitor-.01 microfarad 100 volts glass laminate type.	C108, 109	2
37.	Capacitor-0.02 microfarad 50 volt polycarbonate film type.	C107	1
38.	Capacitor - 5 microfarad 15 volt electrolytic capacitor (tantalum)	C105	1

TABLE 1

PARTS LIST - INVERTER CONTROL SYSTEM (cont'd)

Item No.	Description	Circuit Designation	Quan.
39.	Capacitor - 0.33 microfarad 50 volt polycarbonate film type	C 106	1
40.	Band Pass Filter-UTC No. MNF-O.4		1
41.	Choke, Pulse Engineering Inc. P.N. TH-500	L101	1

TABLE 2
PARTS LIST - SYNCHRONIZING CIRCUIT

Item No.	Description	Circuit Designation	Quan
1.	MC206F dual nand gate by Motorola	1C 401, 415	2
2.	MC202F three input nand gate by Motorola	1C 406	1
3.	MC208F dual nand gate by Motorola	1C 410, 411, 412, 413, 414.	5
4.	MC209F flip-flop by Motorola	1C 402, 403, 404, 405, 407, 408, 409.	7
5.	2N2222 Silicon transistor	Q401, 402, 404, 405, 406	5
6.	2N491B Unijunction transistor	Q403	
7.	1N914B Silicon diode	CR 401 through 414	14
8.	Resistor-4.7K-1/4w - 5%	R401, 402, 415, 416, 421	5
9.	Resistor-1.2K-1/4w - 5%	R405, 406, 407, 408	4
10.	Resistor-1.5K-1/4w - 5%	R403, 404, 413, 414, 410	5
11.	Resistor-1.0K-1/4w - 5%	R417, 418, 419, 420	4
12.	Resistor-750 -1/4w - 5%	R 409	1
13.	Resistor-62 1/4w - 5%	R 412	1
14.	Resistor-18K - 1/2w - 1%	R 411	1
15.	Capacitor - 0.5 microfarad 50 volts-polycarbonate film type	C401, 402, 403, 404	4
16.	Capacitor-0.02 microfarad 50 volts-polycarbonate film type	C405	1

TABLE 2
PARTS LIST - SYNCHRONIZING CIRCUIT (cont'd.)

Item No.	Description	Circuit Designation	Quan.
17.	DOT-25 transformer by UTC	T401, 402	2
18.	Choke, Pulse Engineering Inc. P. N. TH-500	L401	1

TABLE 3
PARTS LIST - DC-DC CONVERTER CONTROL

Item No.	Description	Circuit Designation	Quan.
1.	MC208F dual nand gate by Motorola	1C502, 503	2
2.	MC209F flip-flop by Motorola	1C501, 504	2
3.	2N2222 Silicon transistor	Q502, 505, 507	3
4.	2N491B Unijunction transistor	Q501, 504	2
5.	2N2904 Silicon transistor	Q503	1
6.	2N3409 dual silicon transistor	Q506	1
7.	1N914B silicon diode	CR501 through 514	14
8.	1N751 zener diode	Z501	1
9.	Resistor - 4.7K - 1/4 watt 5%	R504, 519, 520, 523, 524, 512, 513.	7
10.	Resistor - 1.5K 1/2w 5%	R515	1
11.	Resistor - 1.5K 1/4w 5%	R506, 521, 522, 525, 526	5
12.	Resistor - 3.3K 1/2w 1%	R501, 508, 516	3
13.	Resistor - 470 ohm 1/2w 5%	R502, 509	2

TABLE 3
PARTS LIST - DC-DC CONVERTER CONTROL (cont'd.)

Item No.	Description	Circuit Designation	Quan.
14.	Resistor - 62 ohm 1/2w 5%	R503, 507	2
15.	Resistor - 10K 1/2w 5%	R505, 510	2
16.	Resistor - 1K	R511	1
17.	Resistor - 270 1/2w 5%	R516, 517	2
18.	Resistor - 18K 1/2w 1%	R514	1
19.	Resistor - 100 ohm 1/2w 5%	R518	1
20.	Capacitor - .01 microfarad-50 volts polycarbonate film type	C501, 502	2
21.	Capacitor - .002 microfarad-50 volts polycarbonate film type	C504	1
22.	Capacitor - 1 microfarad-30 volt tantalum	C503	1

TABLE 4

PARTS LIST - PWM OUTPUT STAGE -

Power Rating - 500 VA Nominal
750 VA Overload
11.8 amp short circuit

Item No.	Description	Circuit Designation	Quan.	Net Wt. lb.
1.	2N2222 transistor Motorola	Q301, 302, 305, 306, 311, 310, 315, 316, 317, 318, 319, 320.	12	.0125
2.	2N3506 transistor Motorola	Q303, 304, 313, 314.	4	.094
3.	MHT 8822 Transistor Solitron - 20 amp, 325 volt.	Q307, 308, 309, 310.	4	.300
4.	379 D fast recovery 200 PIV - 12 amp rectifiers by Westinghouse.	CR309, 313, 314, 319.	4	.032
5.	379 H fast recovery 400 PIV- 12 amp rectifiers by Westinghouse.	CR310, 311, 316, 317.	4	.032
6.	UTR-31, 1 amp, 300 PIV fast recovery diode by Unitrode.	CR340, 312, 315, 318, 307, 308, 331, 331.	8	.004
7.	IN3007B zeners, 110V-10W Motorola	Z301, 302, 303, 304, 305, 306, 307, 308.	8	0.165
8.	IN914 diode	CR301, 302, 303, 305, 321, 322, 323, 325.	8	.004
9.	UTR-01, 1 amp-50 PIV fast recovery diode by Unitrode.	CR304, 306, 320, 324, 326, 327, 328, 329, 332, 333, 334, 335, 336, 337, 338, 339.		.006

TABLE 4
PARTS LIST - PWM OUTPUT STAGE - (continued)

Item No.	Description	Circuit Designation	Quan.	Net Wt. lb.
10.	Current feedback drive transformer, TRW 306203.	T302, 303, 304, 305.	4	.400
11.	Voltage drive transformer TRW 306200.	T307, 308, 309, 310.	4	.288
12.	Sustain transistor drive transformer, TRW 306201.	T301, T306.	2	.144
13.	Pulse transformer TRW 306202.	SR301, 302.	2	.08
14.	Output choke 1.0 mhy Iss = 4.35 amps I overload = 6.54 amps Is ckt. = 11.8 amps TRW 305743.	L301	1	1.70
15.	Output Filter capacitor 3 ufd - 300 VDC polycarbonate.	C301	1	.15
16.	Resistors 270Ω, 1/2W 5% compositions type.	R301, 305, 312, 305	4	
17.	Resistors 47Ω, 1/2W 5% compositions type.	R302, 306, 311, 316.	4	.014
18.	Resistors 470Ω, 1/2W 5% compositions type	R307, 308, 309, 310.	4	
19.	Resistors 470Ω, 1W compositions type.	R303, 313.	2	.006

TABLE 4
PARTS LIST - PWM OUTPUT STAGE - (continued)

Item No.	Description	Circuit Designation	Quan.	Net Wt. lb.
20.	Resistor 15 ohm - 5 watt noninductive Sprague 453t 1505	R304, 314.	2	.010
21.	Resistor 10 ohm - 3 watt noninductive Sprague 451E 1005	R317, 318, 319, 320.	4	.015
22.	Resistor 22 ohm - 1 watt composition	R321, 324, 327, 333.	4	.012
23.	Resistor 1 ohm - 3 watt noninductive	R322, 325, 328, 331.	4	.015
24.	Resistor 390 ohm - 1/2 watt composition	R323, 326, 329, 332.	4	.004

TABLE 5

PARTS LIST - DC-DC CONVERTER

Power Rating - 555 VA Nominal
833 VA Overload
28±4 Volts Input, 200 Volts Output

Item No.	Description	Circuit Designation	Quan.	Net Wt. lb.
1.	2N2222 Transistor by Motorola	Q201, 202, 203, 207, 224, 226, 227, 228	8	0.009
2.	2N3506 Transistor by Motorola	Q205, 206, 221, 222	4	0.010
3.	FT-34A Transistor by Fairchild	Q204, 208, 223, 225	4	0.055
4.	2N3230 Darlington Transistor by RCA	Q211, 214, 217, 220	4	0.018
5.	2N3263 Power Transistor by RCA	Q204, 210, 212, 213 215, 216, 218, 219	8	0.080
6.	IN914B Silicon Diodes	CR201, 203, 204, 209 256, 258, 259, 260 DB201, 202, 203, 204	24	0.012
7.	UTR-01, 1 amp, 50 volt, fast recovery diode by Unitrode.	CR202, 210, 255, 257	4	0.002
8.	UTR-12, 2 amp, 100 volt fast recovery diode by Unitrode.	CR205, 208, 251, 254, 214, 218, 225, 227, 234, 238, 243, 247	12	0.006
9.	UTR 3305, 3 amp-50 volt fast recovery diode by Unitrode.	CR211, 212, 213, 215, 216, 217, 220, 221, 222 224, 225, 226, 236, 237, 238, 239, 240, 241, 244 245, 246, 248, 249, 250		0.036
10.	IN661 Silicon diode	CR206, 207, 252, 253	4	0.002
11.	IN2835 Zener diode	Z201, 202, 203, 204, 205, 206, 207, 208	8	0.325

TABLE 5

PARTS LIST - DC-DC CONVERTER (Con't)

Item No.	Description	Circuit Designation	Quan.	Net Wt. lb.
12.	Sustain Transistor Drive Transformer TRW Part No. 306223	T 201, 207	2	0.375
13.	Drive Xfmr. TRW 306224	T202, 203, 205, 206	4	1.000
14	Balancing Reactors-2-25 amp coils TRW 306225	BR201, 202, 203, 204	4	0.400
15.	Power Output Transformer TRW 305755	T204	1	1.000
16.	DC Choke, 210 microhenry, 2.7 amps TRW 305741	L202	1	0.700
17.	800 cycle trap choke 2.7 mhy, 2.7 amps TRW 305742	L203	1	.500
18.	DC input choke 10 micro-henry - 26 amp TRW 305753	L 201	1	.250
19.	DC output capacitor 30 microfarad-300 volts (10-3 microfarad-300 volt polycarbonate-Sprague 260p types)	C202	1	1.070
20.	800 cycle trap capacitor 15 microfarad-300 volts (5-3 microfarad polycarbonate-Sprague 260P types)	C203	1	0.535
21.	Input Capacitor-12 microfarad-200 volt (3-4 microfarad-200 volt polycarbonate Sprague 260 P types)	C201	1	0.215

TABLE 5

PARTS LIST - DC-DC CONVERTER (Con't)

Item No.	Description	Circuit Designation	Quan.	Net Wt. lb.
22.	Shunt capacitors-.001 microfarad-200 volt (Sprague 238P poly-carbonate types)	C204, 205, 206, 207	4	0.080
23.	Saturating Pulse Transformer TRW No. 306202	SR 201, 202	2	.080
24.	Resistor-5W-1% non-inductive 7.5 ohm	R203, 233	2	.010
25.	Resistor-3W-1% Non-inductive 10 ohm	R204, 210, 214, 215 219, 220, 224, 225	8	.030
26.	Resistor, 270 ohm, 1/2W 5% composition type	R201, 205, 232, 236 207, 208, 229, 230	8	.010
27.	Resistor-47 ohm-1/2W 5% composition type	R202, 206, 231, 235 211, 216, 221, 226	4	.005
28.	Resistor-470 ohm-1W 5% composition type	R204, R234	2	.006
29.	Resistor-100 ohm - 1/2W - 5% composition type	R213, 218, 223, 228 R212, 217, 222, 228	8	0.010
				6.831

TABLE 6

PARTS LIST - LOGIC AND DRIVE POWER SUPPLY

Item No.	Description	Circuit Designation	Quan.
1.	MC 209 F Flip-Flop by Motorola	1C 601, 602	2
2.	MC 208F Dual Nand Gate by Motorola	1C 603, 604	2
3.	2N2222 Silicon Transistor	Q601, 604, 606, 614	4
4.	2N2904 Silicon Transistor	Q602, 611	2
5.	2N3605 Silicon Transistor	Q612, 613	2
6.	2N491B Silicon Unijunction Transistor	Q603, 605	2
7.	2N3230 Silicon Transistor	Q607, 608, 609, 610	4
8.	Power Transformer TRW P.N. 306243	T601, 602	2
9.	IN 914B Silicon Diode	CR 601 thru 618, 673	19
10.	IN 645 Silicon Diode	CR 623 thru 672	50
11.	UTR-12 , 2 amp-100 volt Silicon Diode	CR 619 thru 622	4
12.	IN 964B Zener Diode	Z 601	1
13.	IN 746 Zener Diode	Z 602	1
14.	IN 751A Zener Diode	Z 603	1
15.	IN 748 Zener Diode	Z 604	1
16.	IN 753 Zener Diode	Z 605, 606	2
17.	Resistor, 1/4W, 5%, 4.7K Composition Type	R601, 606, 607, 610, 611, 616, 617, 623, 624	9

TABLE 6
PARTS LIST - LOGIC AND DRIVE POWER SUPPLY (Con't)

Item No.	Description	Circuit Designation	Quan.
18.	Resistor, 1/4W, 5%, 1.5K Composition Type	R602, 612, 615, 618, 621, 625	6
19.	Resistor, 1/4W, 5%, 10K Composition Type	R603, 604	2
20.	Resistor, 1/2W, 5%, 240ohm Composition Type	R605	
21.	Resistor, 1/2W, 5%, 47 ohm Composition Type	R606, 608, 613, 614, 619, 620	6
22.	Resistor 1/4W, 5%, 120 ohm Composition Type	R622	1
23.	Resistor, 1/4W, 5%, 3.3K Composition Type	R626	1
24.	Resistor, 1/4W, 5%, 2.7K Composition Type	R627, 628	2
25.	Resistor, 1/4W, 5%, 3.9K Composition Type	R629	1
26.	Resistor, 1/4W, 5%, 6.2K Composition Type	R630	1
27.	Resistor, 1W, Wire Wound, 1%, 10 ohm	R632	1
28.	Resistor, 1W, Wire Wound, 1%, 35 ohm	R633, 634	2
29.	Resistor, 1W, Wire Wound, 1%, 27 ohm	R635	1
30.	Resistor, 1W, Wire Wound, 1%, 270 ohm	R636, 637, 638, 639	4
31.	Resistor, 1W, Wire Wound, 1%, 120 ohm	R640, 641, 642, 643	4

TABLE 6

PARTS LIST - LOGIC AND DRIVE POWER SUPPLY (Con't)

Item No.	Description	Circuit Designation	Quan.
32.	Capacitor, .01 mfd-200 volt GE 74F01B-103 (polycarbmate)	C601, 602	2
33.	Capacitor, 6.8 mfd-35 volt Sprague 150D	C603, 604, 605, 610, 611, 612, 613, 614, 615, 616, 617	11
34.	Capacitor, 22mfd, 15 volt Sprague 150D	C606, 607, 608, 609	4
35.	Choke, 1.8 amp, 10 microhenry ACDC Inc. No. RFC-L-10	L601	1
36.	Choke, 1.3 millihenry MCE, Inc. No. OA25FL-21	L602	1

IV. PACKAGE DESIGN

A. SUMMARY

The Static Inverter mechanical design is directed at a finished product that is at once - producible, reliable and functional. Sharing paramount importance with reliability is the aspect of producibility. It has been clearly demonstrated that fabrication ease leads most directly to reliable performance.

The selection of methods of fabrication and the tooling required are the major factors in the end-product reliability for, as in the case of methods of interconnection, it is the reproducibility and inherent reliability of these very techniques that dictate end-product performance.

The functional nature of the finished unit can also be enhanced by its mechanical design. Proper environmental protection, adequate thermal design and structural integrity have been emphasized in the Inverter arrangement. This arrangement has attempted, where possible, to dually interpret functionalization by logically dividing the assembly into testable subassemblies amenable to maintenance.

Although the above attributes have never been traded off against weight or volume, it has been possible through the use of efficient three dimensional packaging techniques to arrange standard components in an efficient overall package design. An integrated, functional design has been proposed rather than one of minimum weight, or volume, achieved at the expense of structure, protection and performance, environmental or thermal margins.

B. GENERAL DESCRIPTION

The Static Inverter is a separable assembly made up of five (5) major subassemblies: (see Figures 20, 21, and 22)

1. PWM Unit
2. DC-DC Conversion Unit
3. Control Electronics Unit
4. Unit Interconnection Module
5. Connector Interface Adapter Module

The three (3) units are stacked vertically and bolted together to form a solid assembly. They are then electrically connected through the attachment of the interconnection module at the rear. The lowermost unit in the stack (the PWM) carries captive mounting hardware for installation of the final assembly

into the spacecraft. A removable EMI cover is shown in the pictorial view of the Static Inverter. The EMI cover is not the humidity protection for the Control Electronics Unit and could be left out of final assembly if EMI environments proved less severe.

Finally, an electrical bonding boss of alodined aluminum with a self-locking insert is provided if installation requires such chassis grounding.

The Connector Interface Adapter Module is attached to the input - output plug on the PWM Unit and provides a means of interfacing with various spacecraft connector types in varying applications of the Static Inverter through the use of a minimum cost replaceable unit.

Synchronization and phasing signals are introduced directly into the Electronic Control Module through the use of R-F connectors. The nature of these signals assures the general use of this common type connector so that no adapter pigtail assembly is included in the Static Inverter design. Obviously, one could be added if a special application required it.

Three (3) phase synchronization signals are given as outputs from each Static Inverter. As only the combined operation of three (3) inverters in a three-phase system would require the use of these outputs, they are plastic-sealed with silastic at final assembly to moisture-proof this interface.

Removable dust closures are shipped with the remaining RF connectors.

C. ENVIRONMENTAL DESIGN

1. Moisture: Protection of the electronics is effected in a combination of methods. Humidity, salt and corrosive atmosphere protection for the main frame of each unit is through the use of 6061-T6 aluminum hardcoat anodized after machining. Although magnesium in these applications would have been two-thirds the weight, the fifty-percent improvement in thermal heat transfer dictates aluminum. This fact, plus the difficulty in adequately finishing magnesium for corrosion resistance in an inexpensive and effective manner, confirms the choice.

   Internal wiring and components are conformal coated with RTV silastic. Each mating surface between units is O-Ring protected to prevent moisture entrapment in the conformally coated wiring areas.

The bottom surface of the PWM unit is for the most part a solid aluminum heatsink with anoidze finish. The areas of wiring channels and component mounting cavities are potted with solid polyurethane (E-1528) applied to a primed aluminum wall to prevent moisture penetration. Because factory repair is required to remove this compound, its use has been restricted to those non-O-Ring protected areas.

2. Shock & Vibration Environments: Shock and vibration environments are easily met without vibration isolators by the solid drill block cordwood construction with the possible exception of the EMI cover. To reduce weight, this optional feature is necessarily thin and may require foam vibration dampers if high frequency resonance develops in qualification. The removable modules in the Control Unit have been angled to include the dampers, if necessary, as well as to reduce module weight. It should again be pointed out that exposed potting on these modules is also hard urethane foam and the EMI cover is not required for moisture protection.

3. EMI: EMI-mechanical considerations have been included in the design. Each separable module has been provided with a pin wired to the metal module frame. In the Electronic Control Unit, the interconnection frame of this unit has a terminal which is electrically bonded to the metal frame, and displayed at the rear of the frame as a unit interconnection pin. It is possible then to tie all metal frames to a common, electrical reference, and through the bond point on the front of the inverter, to tie it in turn to the spacecraft. These are all options which may be included if testing of prototypes indicates their necessity.

   EMI filters of the bulkhead type are provided at the input-output section of the PWM Unit frame. A "clean" area is maintained at the input-output pin area by allowing this bulkhead to extend to the plane of the coldplate and by providing a cover over the connector back.

   An optional EMI cover is available for the Electronic Control Unit. All synchronization signals are handled by separate RF connectors directly accessing the control module, and not internal-routed through the various other stages.

D. THERMAL DESIGN

1. Specifications Assumed: Thermal design of the Static Inverter is based exclusively on conductive cooling through the use of pressure contact with a spacecraft-provided-coldplate. The coldplate mating

surface at the interface with the Static Inverter is assumed to have a minimum thermal conductivity of 100 BTU/hr/ft^2/°F to the coldplate coolant. The maximum coolant temperature is 135°F. Because the maximum operating ambient is specified at 160°F, it is recommended that the EMI cover be gold iridite finished to provide low emissivity thus minimizing the load placed on the coldplates due to ambient temperature rise.

2. Thermal Sensors: The Thermal Sensors are recommended to be bonded in the PWM Unit and DC-DC Converter Unit (see Figure 25 for location). These are hand-wired to the interface input-output connector and are available either as a test point or cable wiring to telemetry.

3. Internal Heat Transfer: Internal heat transfer is dependent on conduction through the unit frames. All high dissipation components are mounted either by bolting with insulation washers directly to the anodized unit frames or by being staked in place with RTV silastic potting compound. Bolt or Stud-mounted-components are subsequently staked to the level of their mounting cavity to provide conduction to the unit frame walls from all surfaces of the component. Over ninety percent of the heat dissipation occurs in the PWM Unit frame which is the base of the finished inverter assembly. This PWM Unit is directly mounted to the coldplate with ten (10) number 1/4-28 UNF bolts. Their spacing is approximately every three inches along each edge of the assembly. The bolt rows are about four inches apart. The size of the bolts and their frequency permit torque and force values to guarantee minimum thermal resistance across the PWM inverter to coldplate interface forming a true pressure joint. The bottom finish of the inverter is maintained at less than 32 micro inches RMS with the runout being held to less than ten-thousandths of an inch over the entire surface. It is recommended that silicone grease be applied at installation of the inverter to further optimize the heat transfer.

4. Heat Flux: The mating surface of the Static Inverter is eighty square inches. Because the thermal transfer ability of the plug area is negligible, the heat flux of 150 watts appears over an area of seventy-five square inches. This yields a flux density of conservative two watts/square inch (see Table 7; worst-case dissipations yield only 2.3 watts/in^2). In the three-static inverter configuration, two-hundred and forty square inches of coldplate are utilized with two-hundred and twenty-five being actually involved in heat transfer to a significant degree.

Major Heat Dissipator & Location	Total Watts Worst-Case Dissipation	Maximum Junction Temperature °C
Electronic Control Unit:		
Integrated Circuits	Negligible	75°C
Low Voltage Power Supply (4 units 2N3230 Darlington)	4 Watts (90% Eff.)	160°C
DC-DC Converter Parts that are Located in PWM Unit as Subassembly Module (See Figure)		
2N3230 Darlington (4)	8 Watts	160°C
2N3263 Power Transistor (8)	80 Watts	160°C
PWM Unit Parts		
MHT 8822 (4)	60 Watts	130°C
379D Diode (4)	20 Watts	-----
Total Watts on Worst-Case Dissipation:	172 Watts	

(Worst-Case Inverter Load 750 VA) (80% Efficiency) = 150 Watts Dissipation

POWER DISSIPATION DATA

TABLE 7

In the prototype phase of the Static Inverter, development of an instrumented thermal model of the PWM Unit will be built to accurately plot the thermal profile across this surface. It is felt from preliminary analysis that no flux densities greater than three watts/square inch will be experienced.

5. Sub-Modules: Table 7 lists allowable junction temperatures for major dissipating components. All of these parts have metal heatsinks with metal conductive paths to the coldplate. All but four watts of these major heat dissipating components are in the unit directly in contact with the coldplate. The DC-DC Converter Power Units, with higher allowable junction temperatures, are epoxy-bonded to a removable heatsink subassembly allowing the use of the flat package version of these units. Figure 24 shows some of the detail of this sub-module. Since this module is screw mounted with a silicone greased interface at the unit frame, it is felt that no thermal hot spot will result. All unit frames are also greased at their metal interfaces during final assembly of the Static Inverter. The application will be controlled by specification to be thin layer wiped on application of optimum thickness to avoid thermal resistance due to excess use of grease.

   Although not listed as major dissipators, all stud-mounted Zeners and many larger value resistors are directly mounted into metal heatsinks. This is done not only to ease fabrication but also to provide reasonably uniform temperatures in any given unit and to minimize vertical gradients across the final assembly.

E. MECHANICAL DESIGN AND FABRICATION FEATURES

In addition to the preceding major sections on environmental and thermal considerations involved in the mechanical design, there are a number of separated, significant factors which influence the approach taken. They are included in this general section in aggregate.

1. Connectors and Connections: The input-output connector is a machined platform on the front of the PWM Unit and is made up of forty-eight (48) male Malco pins* in two (2) adjacent cavities. These are the blade wirewrap type pin set in nylon insulators on 1/8 inch centers. Each pin can easily handle 3 amps; they have been used

   * Malco refers to the general set of blade "tuning fork" connectors originally designed by Malco Manufacturing - Chicago, Illinois.

extensively in many missile and spacecraft electronic assemblies. By selecting nickel for the blade material, excellent welds can then be made directly to the pins. Bussing of several pins provides current handling capacity with redundancy possible. The connector area is O-Ring-sealed when the interface adapter module is installed. Non-symmetric dowels assure proper orientation of this module. The interface adapter module displays test points at its top surface. These test points carry electrical short circuit protection in the adapter module and then mate with appropriate pins on the input-output connector. When three (3) inverters are used in parallel, the interface adapter assembly is common to all units if the side-by-side installation is possible. Test points for each inverter may then be wired to one convenient area. Note that such variations do not affect the basic Static Inverter Assembly design.

Male Malco pins are also used at the rear of each unit frame to accomplish the unit-to-unit connections. These also are O-Ring-sealed when the Interconnection Module Assembly is installed. The third application of this connector is in the Electronic Control Module which features pluggable field replaceable modules. O-Ring sealing is obtained interfacially when these modules are plugged. Electrical connections, within a given unit or module, are predominantly welded joints. This technique provides a high strength and extremely reliable connection. Where component configurations are incompatible with this technique, such as the solder lugs normally found on stud-mounted devices, the use of solder per NASA type qualification is specified. Welding has been specified for the wirewrap terminals on the Malco pins not because of unreliability of the wire-wrapping technique but because of the desire to minimize the volume allocated to interconnections. This is commonly done and is a highly reliable technique.

With the exception of the micrologic module, the interconnection approach will be point-to-point welded ribbon wiring using teflon-sleeved nickel. Gold-plated Dumet wire will be used where soldering is required at one end. Interconnections in the micrologic module will be through multilayered printed circuit boards.

2. Unit Frame Construction: The PWM and the DC-DC Converter Units are built in the so-called drilled block method of cordwood construction. A solid piece of aluminum is machined to the exact outside configuration of the finished unit including mounting holes and sealing surfaces. It is then drilled to accept the installation of all large components or module mountings of subassembled groups of components. Areas for making of weld connections and wire runs

are mil-profiled to depth from the top and bottom. Normally, all of this machining can be accomplished on tape-controlled milling machines at nominal cost. After addition of anodize or other finish protections, parts are mounted either by bolting directly or by staking them in position with RTV silastic. Interconnecting wiring is then done followed by testing, potting and then unit testing. Usually the drilled block is its own potting mold as well as being its own assembly jig. A third and prime advantage is that it provides a minimum thermal resistance path in the conductive cooling of components. This is the prime reason for its use in these modules. Its structural ruggedness approaches that of solid metal.

The Electronic Control Unit, because of its lower power dissipation and variety of module types, is of more conventional welded module construction. The unit frame is a thinner assembly machined to final outside configuration with its internal, lower side cored out for large amounts of signal wiring. Holes are then drilled in accurate location by tape control for installation of the large number of Malco pins found in signal logic devices. The pin configuration at the rear of the frame is identical to the other unit frames for the installation of the Unit Interconnection Module Assembly.

RF connectors are installed at the front of the unit for the handling of the synchronization inputs and outputs. O-Ring seals on each module mate with the frame top surface; jacking hold-down inserts are also installed here.

Pin-to-pin wiring in the unit frame is hand-wired with resistance welded connections. While the number of connections is larger than the other unit frames, it is not felt wirewrapping on automatic equipment is necessary and therefore not proposed. There is a resulting economy on overall height.

After wiring, the frame may be hi-pot and continuity-tested then potted with closed cell urethane foam.

3. Spacecraft Installation: Spacecraft installation is proposed to be hard mounted by ten (10) 1/4-28 stainless steel hold-down screws. These screws are captive in the Static Inverter assembly and are spring-retractable when not engaged to ease installation and prevent damage to the mounting finish as the unit is slid along the mounting surface. The hole spacing is approximately every three inches to minimize thermal interface losses. Obviously, the demands of the thermal design guarantee structural security as well. It is assumed that self-locking inserts are provided by the coldplate and that no locking features are furnished with the bolt. It is possible

to install a tapped insert in the through holes that accommodate the mounting bolts of a size that will permit clearance for the mounting bolt and also permit the mount to be made from below the coldplate.

4. Subassembly Functionalization: The mechanical allocation of electronics to the various units and modules within these units is based on several engineering trade-offs. In conductively cooled design such as the Static Inverter, the thermal dissipations of the various circuit elements are of prime importance in functionalization of the subassemblies.

   It is extremely desirable that the prime heat dissipators be low relative to the coldplate to reduce thermal interfaces between units and increase the efficiency of the thermal transfer. For this reason, the PWM stage together with the power transistors found in the DC-DC Converter are placed in the lower unit next to the coldplate (see Figure 24 for details of this module). The remaining portion of the DC-DC Converter is in the next unit layer and, finally, the low voltage power supply and signal level control units are in the upper unit layer most remote from the coldplate.

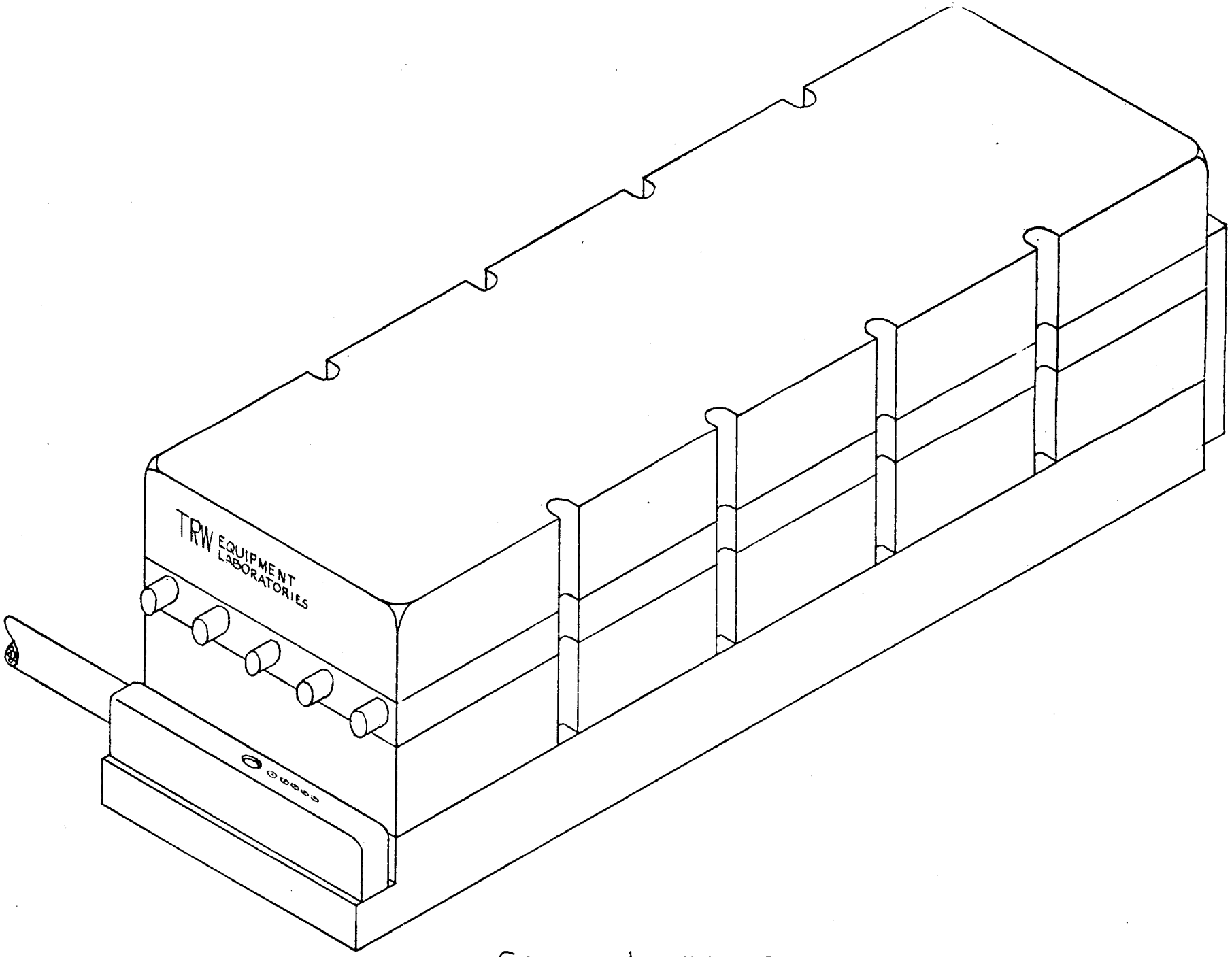
5. Signal Flow: A second and, in some cases, equal consideration in the mechanical division of the system such as this is the Signal Level and Information Flow experienced within the system. Noise and coupling can be reduced if an organized information flow is adhered to. If the synchronization and phasing is removed, the PWM Inverter requires DC power in, and AC power out passing through both the PWM and the DC-DC unit. Power level signals are then confined to the first two unit layers and input (DC) and output (AC) are on opposite sides of these module connectors. Synchronization signals are brought in independently directly to the third unit layer at signal power level. The signal information flow is then a low signal level throughout the top unit. The higher power level is found in the lower two units.

   A fringe benefit from such mechanical organization is that the top accessible layer (access in-field after installation) can be made to have pluggable modules thus allowing some field maintenance and repair. The power stages, because of location and methods of assembly, would require factory maintenance. The pluggable module also has a second feature in that common parts, in terms of form factor such as capacitors and ICs, may be grouped in common modules. This allows many similar units to share a common mounting, a common testing and a common fabrication method at assembly. Such groupings are made in the case of capacitors in the

DC-DC converter and with the micrologic in the control electronics. The remaining modules in the Electronic Control Unit are functionally testable either as completed modules or when plugged into the unit frame with the micrologic module and power supply. In such an approach, it was possible in the case of the DC-DC Converter Unit to realize a volume economy by using fewer of a larger value of capacitor in the output and 800 cps trap capacitor.

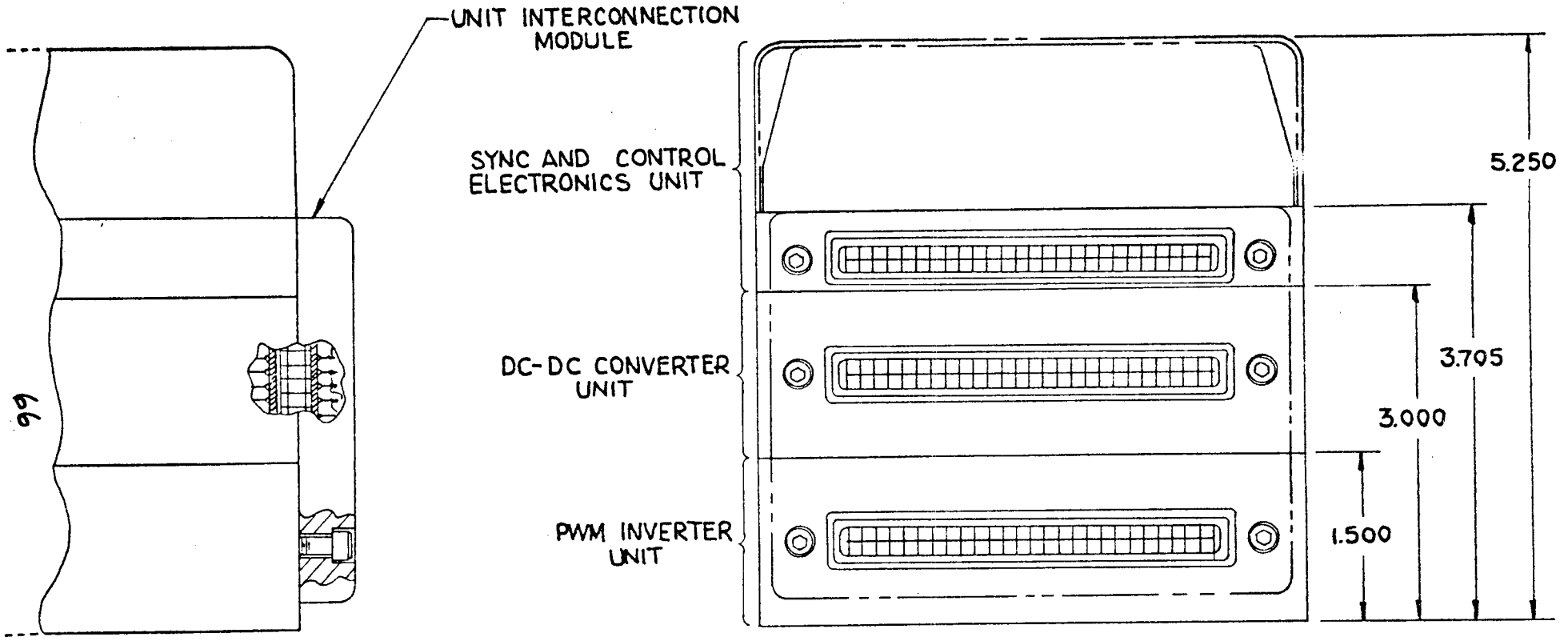
It is recommended that, in the Prototype Unit, certain parts be reoperated and that they be recased by the manufacturer. These are: the IN 2835 Zener Diode found in the DC-DC converter. (The flange on the stud is unnecessarily large for the drilled block mounting.) and the Solitron Transistor in the PWM Unit requires its stud mounting to be shortened to minimize the overall unit height.

6. Weight Volume and Package Efficiency: As indicated in the introductory remarks, the reliability and producibility aspects of the design have been given the prime emphasis. Weight and volume have evolved as a result of these factors while still employing efficient package techniques. The resulting volume is 434 cubic inches total envelope and 400 cubic inches total package. It is estimated that the completed package will weigh 20-22 lbs. exclusive of the Interface Adapter Module. A density factor slightly greater than that of water is indicated (welded module construction yields a density on the average of that of water).



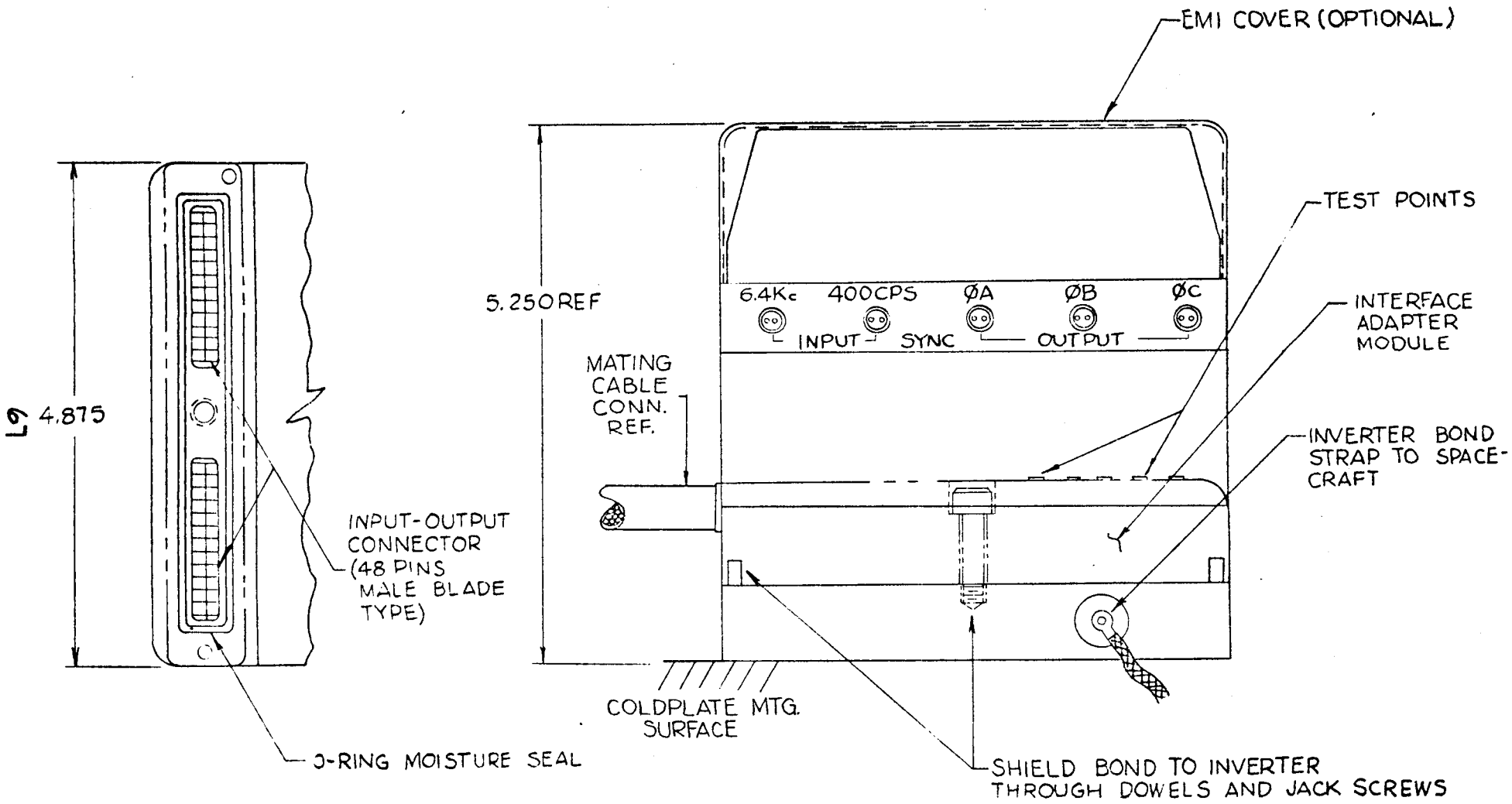
STATIC INVERTER

FIG. 20



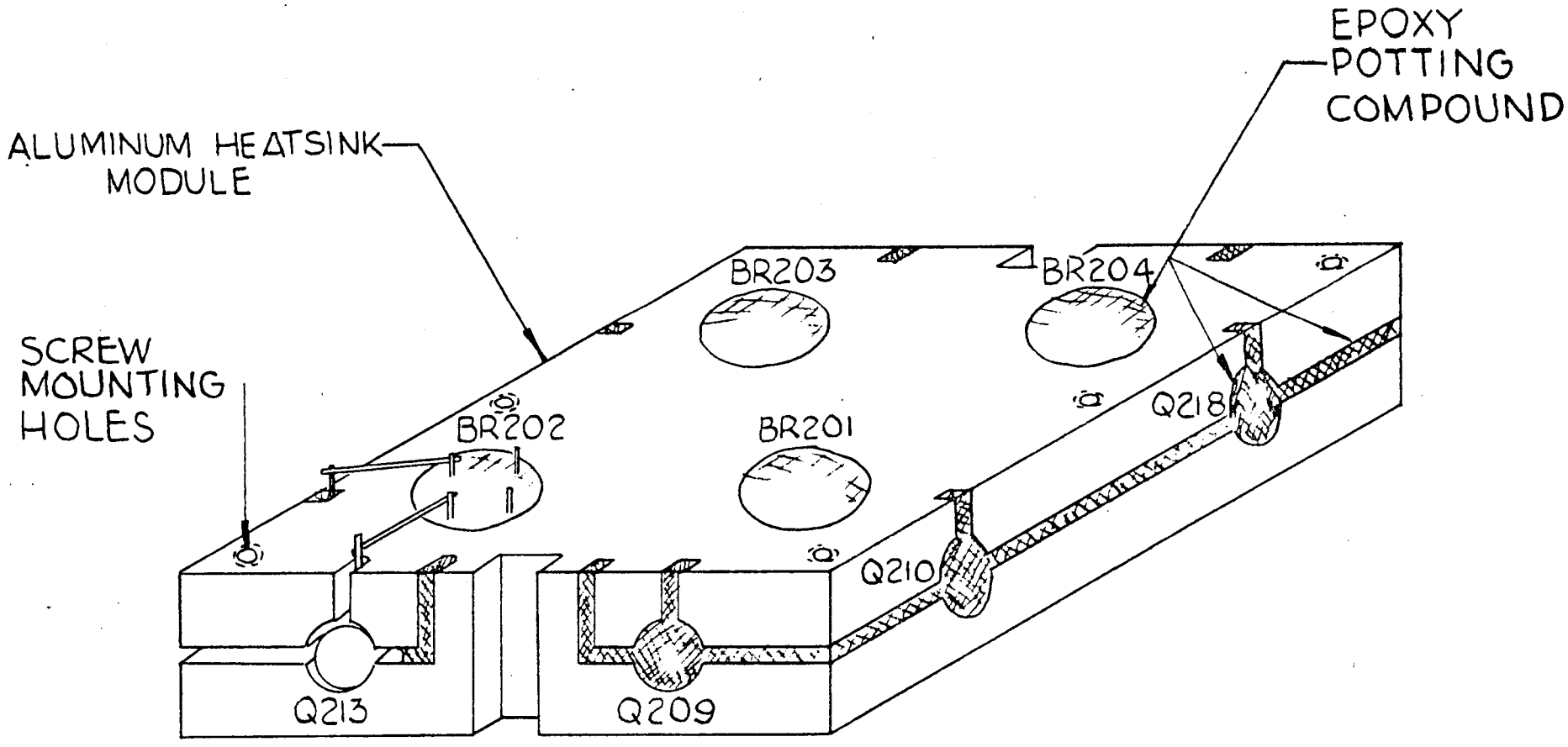
REAR INTERCONNECTION DETAIL

FIG. 21



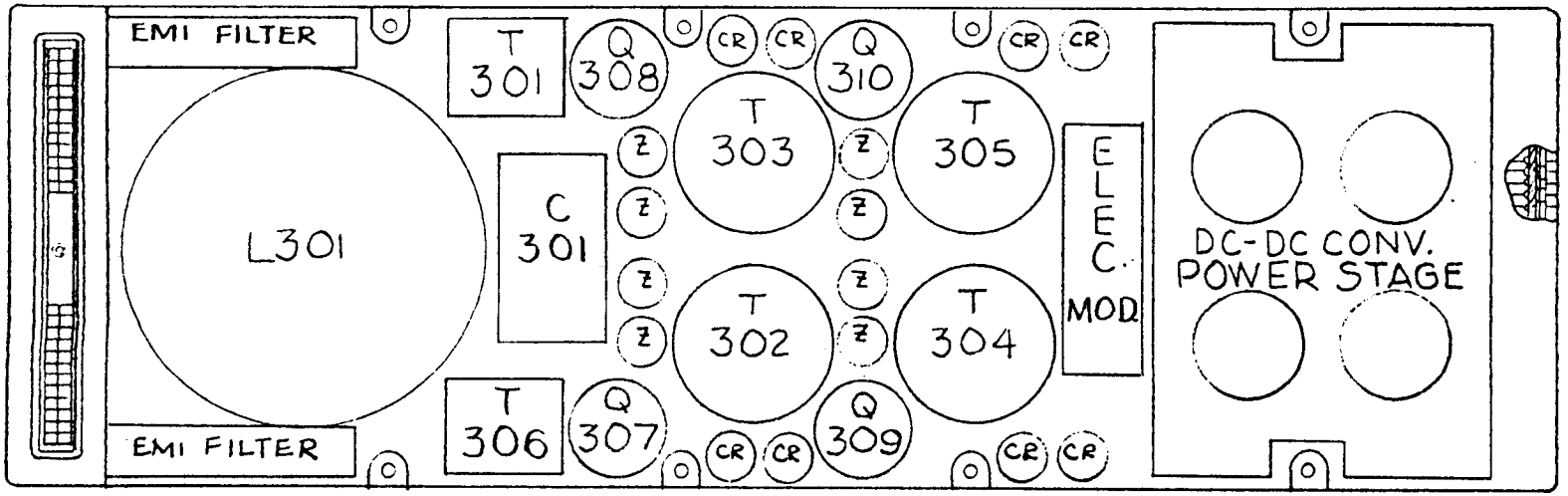
INVERTER INPUT-OUTPUT DETAIL

FIG. 22



DC-DC POWER STAGE MODULE

FIG. 23



PWM INVERTER UNIT

FIG. 24

V. RECOMMENDATIONS AND SUGGESTIONS

It is recommended that the Phase II portion of the Static Inverter Development program be initiated. The Phase II program will verify the designs established in Phase I and provide a prototype inverter package.

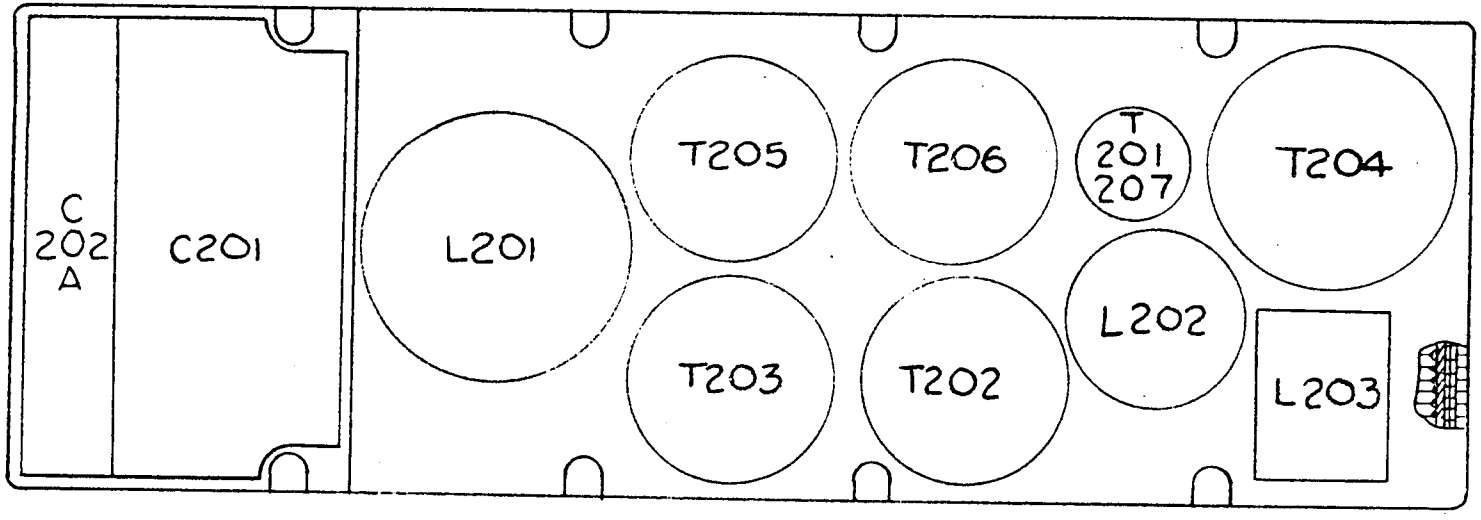
The initial prototype development work can be more effectively performed if the preliminary package design is used when breadboarding the power handling inverter sections. This technique will yield more relistic thermal information and eliminate a step in the transistion from the circuit diagram to the finished prototype.

APPENDIX I

Typical module construction pictorials are included in this appendix. These are mounted by jacking screws captive in each unit into the connectors provided in the Electronic Control Module Frame.

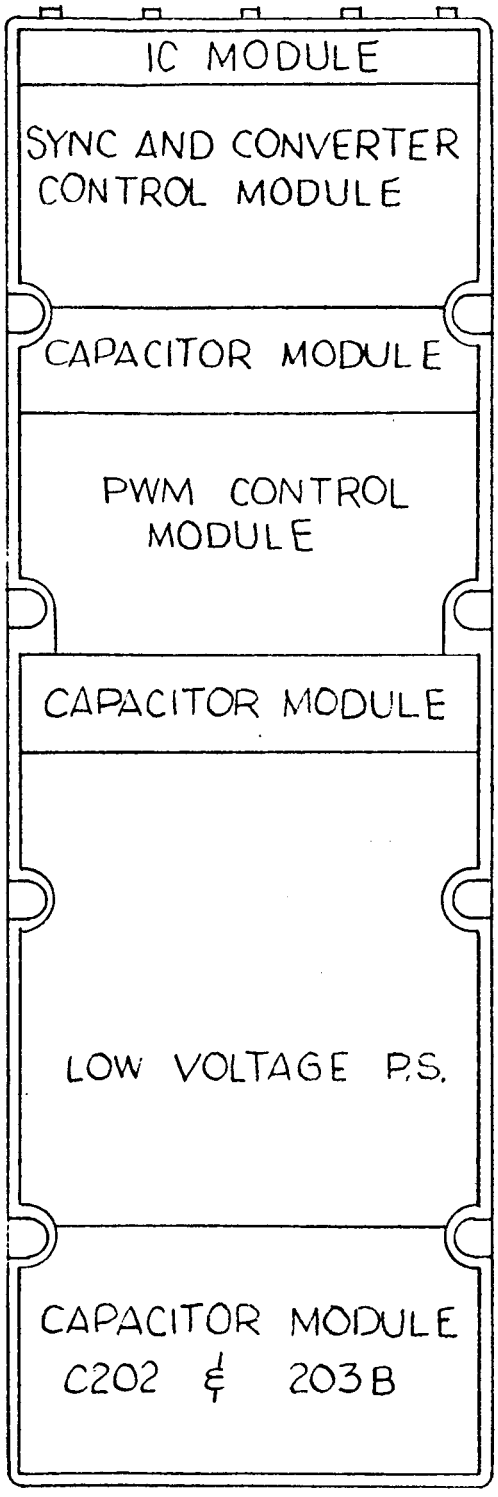
General arrangements of the DC-DC Converter Unit and the PWM Unit are also shown as reference.

In general, these are solid aluminum blocks machined to accept components and wiring.



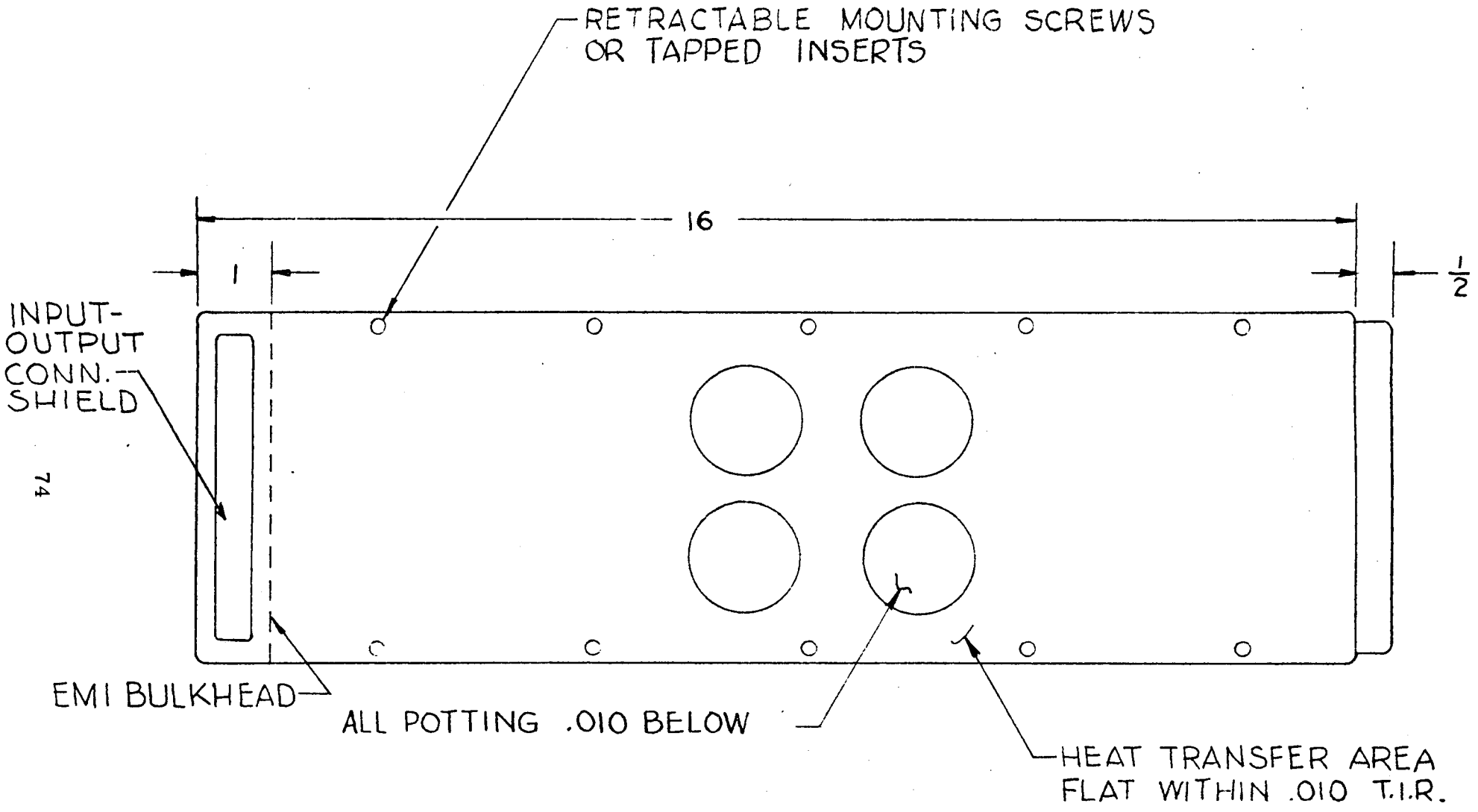
DC-DC CONVERTER UNIT

FIG. 25

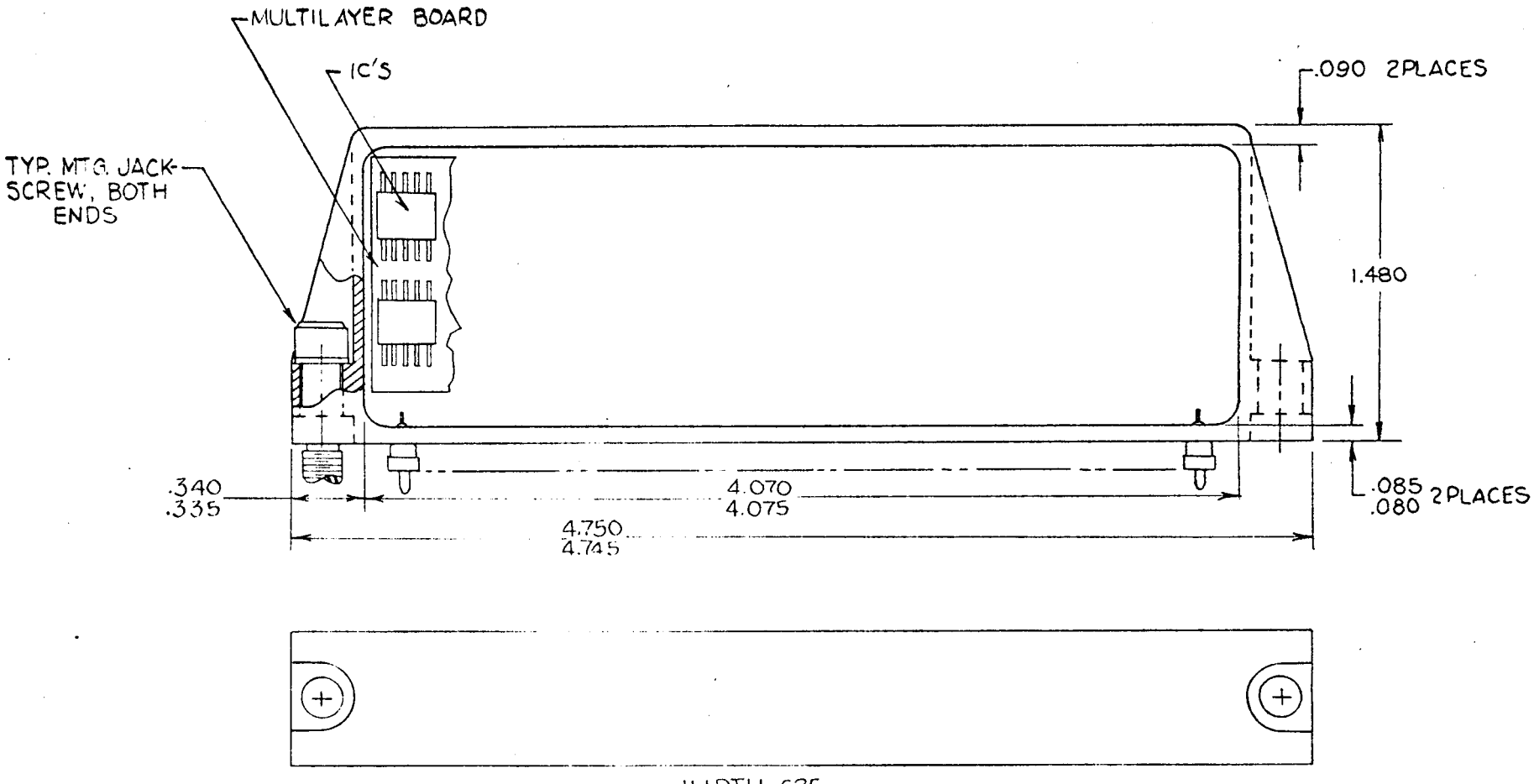


ELECTRONICS CONTROL UNIT

FIG. 26

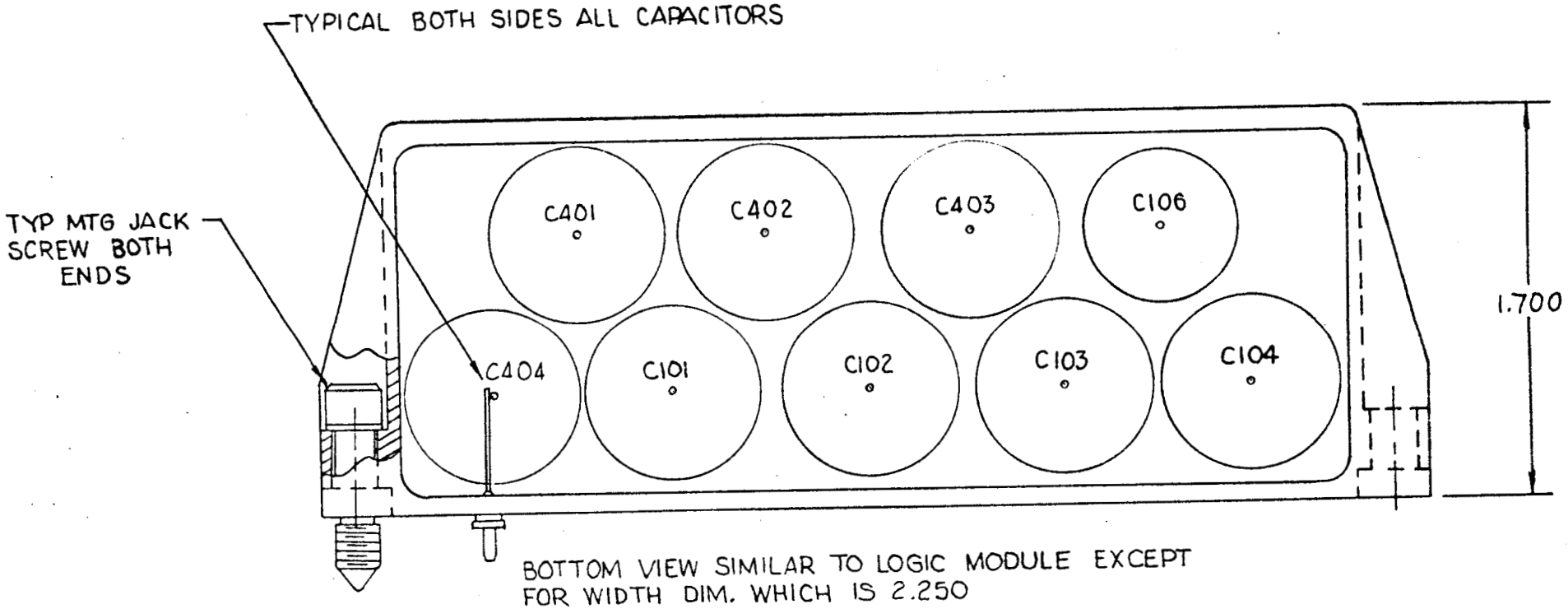


STATIC INVERTER
(BOTTOM VIEW)
FIG. 27



I.C. (INTEGRATED CIRCUIT) MODULE

FIG. 28

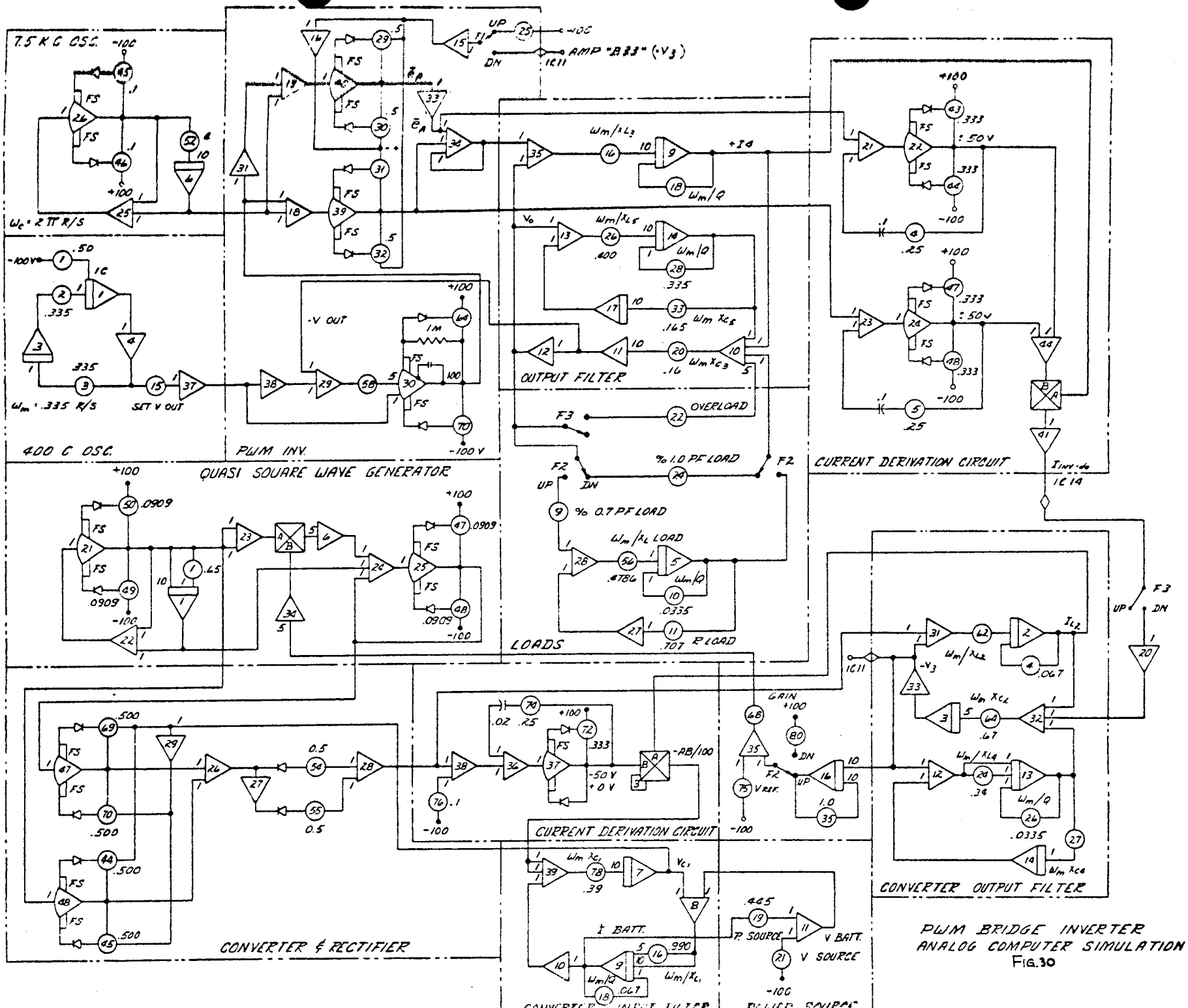


PLUGABLE CAPACITOR MODULE

FIG.29

APPENDIX II

Enclosed in this appendix is an analog computer diagram and a Design Specification extracted from the NASA Work Statement.



PWM BRIDGE INVERTER
ANALOG COMPUTER SIMULATION
FIG. 30

5.0 DESIGN SPECIFICATION

5.1 Introduction - The Design Specification will be divided into two sections as follows:

5.1.1 Design Goals

5.1.2 Design Requirements

5.2 Design Goals - The following goals are submitted for guidance only and should be exceeded if possible

5.2.1 Efficiency

a. 80 percent at full rated load
b. 60 percent at 0.4 times full rated load

NOTE: Full rated load - 500 volt amperes per module based on three modules per three-phase inverter or 750 volt amperes based on 2 modules per three-phase inverter.

5.2.2 Weight - 15.0 pounds per module maximum based on 3 modules per three-phase inverter or 22 1/2 pounds per module based on 2 modules per 3-phase inverter.

5.2.3 Dimensions - To be determined.

5.2.4 Acoustic Noise - The generated acoustic noise shall be below the following levels:

a. Sound Pressure Level: 65 db max broadband noise from 20-10,000 cps.
b. Speech interference Level: 40 db max.

5.2.5 Reliability - The inverter shall be designed to achieve a reliability of 0.960 based on 400 hours of operation at the environments specified herein.

5.3 Design Requirements

5.3.1 Mission Life - The inverter shall be designed to have a total mission life of 1200 hours of operation.

5.3.2 Factor of Safety - Each electrical element within the inverter shall be rated to withstand abnormal parameter variations up to 1.5 times normal rated levels.

5.3.3 Electrical Characteristics

5.3.3.1 Input Voltage - 28 volts DC plus or minus 4 volts.

5.3.3.2 Input Ripple - Less than 1.5 volts RMS as per MIL-STD-704, Paragraph 5.2.2.

5.3.3.3 Input Transients - Inverter shall withstand 80 volts DC for 10 microseconds, and 40 volts DC for 1 second without damage.

5.3.3.4 Turn-On Transient - The turn-on transient after two milliseconds from turn on with the input voltage as specified in 5.3.3.1 and full rated load and power factors shall not exceed 300 per cent of the steady state value for the same conditions. Stabilization to within 10 per cent of the steady state values of input current and output voltage shall occur within 100 milliseconds. The inverter shall stabilize to the performance conditions of this specification within 5 seconds after turn on under all rated combinations of line, load, and environment.

5.3.3.5 Loss of Input Power - No detrimental effects shall occur due to instantaneous removal of input power during operation.

5.3.3.6 Three-Phase Output Voltage - 115 volts RMS plus or minus 1 per cent line to neutral (3-phase, 4 wire system) over rated load, input, and environmental conditions.

5.3.3.7 Output Voltage Transient - The output voltage shall remain within 115 VRMS plus or minus 10 per cent for any step load or line change within the specified normal limits. Recovery to steady state limits shall be within 0.05 seconds. Transient voltage in excess of 225 volts peak shall not appear at the output under any condition.

5.3.3.8 Output Voltage Modulation - As per MIL-STD-704, paragraph 5.1.3.6 except that maximum amplitude shall not exceed 2.0 volts peak.

5.3.3.9 Output Frequency Modulation - The output frequency modulation shall not exceed 0.5 cycles cycles per second under any load and power factor combination specified herein.

5.3.3.10 Load - 0 to 500 volt amperes (V.A.) per modules based on 3 modules per each 3-phase inverter or 0 to 750 V.A. per module based on 2 modules per each 3-phase inverters.

5.3.3.11 Power Factor

a. All load levels: 0.65 lagging to 0.80 leading.
b. 0 to 30 per cent of rated load: 0.80 to 0.1 leading.

5.3.3.12 Overload - The inverter shall be capable of withstanding a 150 per cent overload for a 10 minute period while supplying an output voltage within the limits of paragraph 5.3.3.6, and a 14.0 ampere overload for a maximum of 20 seconds without damage. The inverter shall automatically limit the output current to 14.0 amperes maximum and return the unit to operation automatically upon the removal of the overlaod.

5.3.3.13 Frequency

a. External Synchronization: 400 cps plus or minus 1 per cent.
   Signal Characteristics:
   1. Frequency: 6400 pps.
   2. Duty Cycle: 50 per cent plus or minus 1 per cent.
   3. Amplitude:
      Pulse "on": +3.0 volts plus or minus 0.5 volts.
      Pulse "off": 0 volts plus 0.5 minus 0 volts.
   4. Frequency Stability: 10 parts per million.
   5. Source and inverter impedances: 100 ohms plus or minus 10 per cent.
   6. Rise Time: 1.0 microsecond.
   7. Decay Time: 1.0 microsecond.
b. Free-Running Mode: 400 cps plus or minus 2 per cent.

5.3.3.14 Waveform - As specified in MIL-STD-704, Paragraph 5.1.3.5.

5.3.3.15 Isolation - The AC output and DC input shall be electrically isolated from each other and from the case except for Radio Frequency Interference feed-through capacitors which may be grounded to the case. No breakdown shall occur when 400 volts DC is applied between the input power terminals and the inverter case, and 750 volts DC between the AC output terminals and the case.

5.3.3.16 Ripple Generation - The inverter shall not superimpose onto the DC input line any voltage in ex excess of 0.5 volts peak between DC and 15 KC when measured across an input source with an impedance of 500 milliohms.

5.3.3.17 Motor Starting - The inverter shall be capable of starting an induction motor load while simultaneously supplying 60 per cent of its rated output. The motor load shall be simulated by connecting two fans (Rotron Manufacturing Company Type AXIMAX-3, single phase, motor series 528YS) in parallel across the output and disconnecting one of the fans after 5 seconds. The fans shall be simultaneously started.

5.3.3.18 Parallel and Three Phase Operation - The individual single phase inverters shall be capable of being interconnected for any combination of parallel and/or three phase operation.

5.3.3.19 Electromagnetic Interference - The equipment shall meet the design, quality assurance, testing, and documentation requirements of MIL-I-26600 and MSC addendum ASPO-EMI-10A. In case of a conflict in specifications, the tests and requirements specified in MIL-I-26600 and MSC addendum ASPO-EMI-10A shall not be superseded by any other test or requirement included in these specifications.

5.3.3.20 Dielectric Strength - Electrical parts and subassemblies prior to being wired shall be capable of withstanding an electrical potential of 1500

volts RMS, 60 cps in accordance with MIL-STD-202, Method 301 between insulated points and case without electrical breakdown. Criterion of Failure:

a. Breakdown, or
b. Current flow in excess of 500 microamps.

All items which cannot be tested for dielectric strength will be subject to approval.

5.3.3.21 Protective Devices - Protective devices which require replacement or manual resetting shall not be used.

5.3.4 Mechanical Characteristics

5.3.4.1 Thermal Requirements

a.

a. The major heat-dissipating elements of the power inverter shall be mounted on a heat sink, one surface of which shall be exposed on the module for external conduction cooling. For design purposes the inverter assembly shall be considered thermally isolated from all conducting structures. Spacecraft mounting surface will have at least 200 square inches of contact area.

b. Heat Flow - Maximum allowable heat flux in any portion of the inverter: 3.0 watts per square inch.

c. Thermal Conductivity - Heat sink to cold plate: 100 BTU/hr/ft^2/°F

d. Heat sink surface:
Finish: 32 microinches RMS max.
Flatness: Within 0.010 inches total indicated run out.

5.3.4.2 Sealing - The inverter shall be designed such that those portions of the circuit that will burn, spark, or outgas because of electrical overload or short circuit are hermetically sealed or potted. Potting must be of the closed-cell foam type which will not support combustion.

5.3.4.3 Vibration Isolators - The inverter shall be designed such that vibration isolators will not be required.

5.3.5 Environmental

5.3.5.1 Temperature Limits

a. Operating Ambient: 0-160°F
b. Cold Plate Coolant Temperature: 35°F min to 135°F max.

5.3.5.2 Temperature Sensors - Temperature sensors shall be incorporated at critical points to provide an external indication of excessive temperature conditions. The temperature sensors shall be provided as shown necessary by the reliability and maintainability studies to be performed during the Development Stage.

5.3.5.3 Thermal Vacuum - The inverter will be exposed to a vacuum of 1.0×10^{-5} millimeters Mercury. The unit will be operated at full load over the ambient temperature range given in 5.3.5.1a.

5.3.5.4 Shock - The unit will be capable of withstanding a peak acceleration of 20g. The chock pulse waveform will be a saw tooth with an 11 millisecond rise time and a 1 millisecond decay. The unit will be operating during this test and will be expected to remain within specified tolerances.

5.3.5.5 Vibration

a. Sinusoidal: 5-100 cps - Linear increase from 0.3g at 5 cps to 8.5g at 100 cps.
100 - 300 cps - 8.5g
300 - 2000 cps - Linear decrease from 8.5g at 300 cps to 5g at 2000 cps.
Sweep Rate: 1/2 octave perminute for 2 cycles in each of three mutually perpendicular axes.

b. Random: 20 - 95 cps - 0.041 g^2/cps
85 - 100 cps - 12db/oct rise
100 - 1000 cps - 0.078 g^2/cps
1000 - 1200 - 12 db/oct roll-off.

1200 - 2000 - 0.041g^2/cps.

Vibration in three mutually perpendicular axes, 17 minutes in each axis.
Ambient temperature: 160°F
Inverter will be operated and shall remain within specified tolerances.

5.3.5.6 Acoustic Susceptibility - The inverter shall be capable of withstanding a sound pressure level of 140 db overall with a frequency range of 4.7 to 9,600 cps.

5.3.6 Test Points - An adequate number of test points shall be provided for each subassembly to facilitate isolation of faults in the inverter.

APPENDIX III

This section contains the winding data for the wound components that are not available from commercial stock.

Part No.	Description	Core	Coil No.	Winding Data
306222	Current transformer	50000-2A by Magnetics, Inc.	Primary Secondary	1000 turns #35 wire 2 turns of 5 #20 wires
306203	Current feedback drive	C1300D215A cup with T1300D240 cover by A-B.	N_c N_b N_f	15 turns of 5 #30 wires 8 turns of 3 #25 wires 1-1/2 turns of 20 #25 wires
306200	Voltage drive transformer	C1000D295B cup with T1000D151A cover by A-B	N_s N_b	150 turns of #30 wire 50 turns of #30 wire
306201	Sustain transistor drive transformer	EE-24-25 4 mil alloy 48 lamination (Magnetic-Metals, Mag-netics, Inc. etc)	N_{p1} N_{p2} N_{c1} N_{c2} N_{b1} N_{b2}	120 turns #32 wind bifilar 120 turns #32 43 turns #32 wind bifilar 43 turns #32 35 turns #32 wind bifilar 35 turns #32
306202	Pulse transformer	80523-1/2DMA Magnetics, Inc.	N_p N_{s1}, N_{s2}	36 turns #30 wire 9 turns #30 wire each
305743	Output Choke	A-124030-2 by Arnold	N	182 turns of 2 #17 wires
306223	Sustain transistor drive transformer	T-0620D101A by A-B	N_{p1} N_{p2} N_{b1} N_{b2} N_{c1} N_{c2} N_{h1} N_{h2}	105 turns #32 wind bifilar 105 turns #32 30 turns #32 wind bifilar 30 turns #32 39 turns #32 wind bifilar 39 turns #32 42 turns #32 wind bifilar 42 turns #32

Part No.	Description	Core	Coil No.	Winding Data
306224	Drive transformer		N_s	106 turns of #30 wire
			N_c	100 turns of #22 wire
			N_f	2 turns of 28 #20 wires
			N_{b1}	40 turns of 2 #21 wires
			N_{b2}	40 turns of 2 #21 wires
306225	Balancing Reactors	T-0620D101A by A-B	N_1	3 turns of 8 #20 wires
			N_2	3 turns of 8 #20 wires
305755	Power Output transformer	T2400D208A cup with C2400D207A cover	N_p	8 turns of 17 #21 wires
			N_s	83 turns of 2 #21 wires
305741	DC Choke	2No. 55076-A2 by Magnetics, Inc.	N	62 turns of 5 #22 wires
305742	800 Cycle trap choke	Arnold No. AZ55 C-Core with gap of glass-epoxy grade g-10	N	120 turns of #16 wire
305753	DC Input Choke	Air	N	16 turns of .032 x .640 alum. strip interleaved with .002 mylar. I.D. is 1.300 in. and O.D. is 2.58 nominal.

Part No.	Description	Core	Coil No	Winding Data
306243	Power Transformer	52004-1/2A By Magnetics, Inc.	N_{p1}	317 turns #25 Wind bifilar
			N_{p2}	317 turns #25
			N_1	114 turns of 2 #23 wires
			N_2	30 turns of 2 #27 wire
			N_3	45 turns of #30 wire
			N_4	45 turns of #30 wire
			N_5	10 turns of #32 wire
			N_6	114 turns of #32 wire
			N_7	114 turns of #32 wire
			N_8	114 turns of #32 wire
			N_9	114 turns of #32 wire
			N_{10}	114 turns of #30 wire
			N_{11}	114 turns of #30 wire
			N_{12}	114 turns of #30 wire
			N_{13}	114 turns of #30 wire